Study of the Digital LLRF System for STF*

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Abstract STF is a test facility for ILC which is under construction in KEK, Japan. The digital LLRF system is used to control the RF phase and amplitude inside the superconducting cavities. Because there is no real cavity to be controlled, a real time cavity simulator is designed to simulate the cavity response. An FPGA based cavity controller is designed to control the cavities. In the FPGA program, PI feedback and feed forward algorithm are adopted. Measurement shows that both the cavity simulator and the cavity controller work well.

Key words digital LLRF, FPGA, cavity simulator, STF

1 Introduction

STF (Superconducting RF Test Facility) is a test facility for ILC (International Linear Collider) proposed by KEK from the year of 2004.

STF employs a superconducting cavity as the accelerating structure. The basic RF frequency is 1.3GHz and the pulse width is 1.5ms with a repetition frequency of 5Hz. The flat top of the RF pulse with beam is about 1ms. During the flat top, the RF amplitude stability should be less than $\pm 0.3\%$ (rms), and the RF phase stability less than $\pm 0.3^\circ$(rms)[1].

To meet the requirements for RF stability, the digital LLRF system based on FPGA is used to control the RF phase and amplitude. FPGA (Field Programmable Gate Array) is suitable to do fast digital signal processing, which can perform the control algorithm within several hundred nanoseconds. In the FPGA, PI feedback and feed forward algorithm are adopted[2]. For STF phase-1, eight cavities will be installed, and the RF vector sum of these cavities will be controlled by the digital LLRF system.

Because the superconducting cavity is not ready to be operated with RF power, a real time cavity simulator is implemented into another FPGA to play the role of a real cavity. The cavity simulator can be used to evaluate the performance of the control system and also can be used to train the operators, avoiding the possibility of destroying hardware.

The simplest diagram of the LLRF system with cavity simulator is shown in Fig. 1.

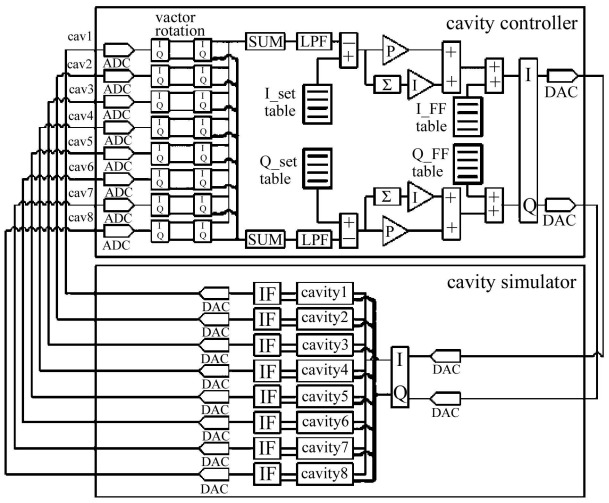

Fig. 1. Block diagram of the STF LLRF system.

Received 10 November 2006, Revised 4 January 2007
* Supported by National Natural Science Foundation of China (10575115) and JSPS
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2 Cavity simulator design

2.1 Cavity voltage equation[3]

The superconducting cavity can be modeled as an RLC resonance circuit, which is shown in Fig. 2.

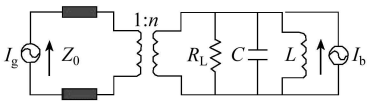

Fig. 2. The cavity model.

where I_g is the driving current corresponding to the RF injection power, R_L is the loaded resistance, and I_b is the Fourier component of the beam current at the operating frequency of the cavity.

The base band real and image components of the cavity voltage will follow the equation of

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} V_r \\ V_i \end{bmatrix} = \begin{bmatrix} -\omega_{1/2} & -\Delta\omega \\ \Delta\omega & -\omega_{1/2} \end{bmatrix}\begin{bmatrix} V_r \\ V_i \end{bmatrix} + R_L\omega_{1/2}\begin{bmatrix} I_r \\ I_i \end{bmatrix}, \tag{1}$$

where $\omega_{1/2}$ is the bandwidth of the cavity, $\Delta\omega$ is the detuning of the cavity. And the current will include both the driving current I_g and the beam loading I_b.

2.2 Lorentz force detuning

When the superconducting cavity is running in pulsed mode, the mechanical oscillation will be driven by the Lorentz force generated by the large magnetic field and the wall current.

The Lorentz force will drive several mechanical resonance modes and for the mth mode

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} \Delta\omega_m \\ \Delta\dot{\omega}_m \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -(2\pi f_m)^2 & \dfrac{-2\pi f_m}{Q_m} \end{bmatrix}\begin{bmatrix} \Delta\omega_m \\ \Delta\dot{\omega}_m \end{bmatrix} + 2\pi V^2\begin{bmatrix} 0 \\ -K_m(2\pi f_m)^2 \end{bmatrix}, \tag{2}$$

where f_m is the resonance frequency of the mth mode, Q_m is the quality factor and K_m is Lorentz force detuning constant, and V^2 is the square of the cavity voltage. The total detuning is the sum of the detuning caused by each mechanical mode.

2.3 Implementing the cavity simulator

The block diagram of the cavity simulator is shown in Fig. 3, which is made by the software of System Generator. The cavity is driven by the injection RF power and the beam current, and the cavity voltage will drive the mechanical oscillation which will cause Lorentz force detuning. And the detuning will finally influence the cavity voltage backward[4].

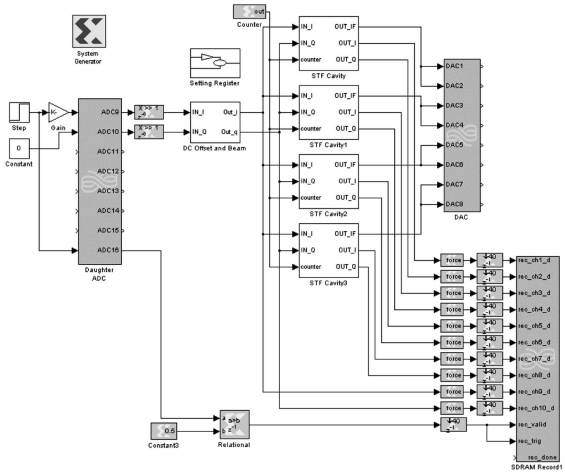

Fig. 3. FPGA program for the cavity simulator.

The cavity simulator is implemented in an FPGA board. For the first version, XtremeDSP board with one FPGA chip (Virtex-IV), two 14bit ADCs and two 14bit DACs is used. And for the latest version of the cavity simulator, a VHS-DAC board form the company of LYRTECH is used, which has one FPGA chip (Virtex-II), eight 14bit ADCs and eight 14bit DACs. So, the new version of the cavity simulator can simulate at most eight cavities with one single FPGA board, which is shown in Fig. 1.

The step response can be used to evaluate the performance of the cavity simulator. The base band step response of the cavity simulator including both the electrical and mechanical model is shown in Fig. 4, from which the effect of Lorentz force detuning can be observed obviously.

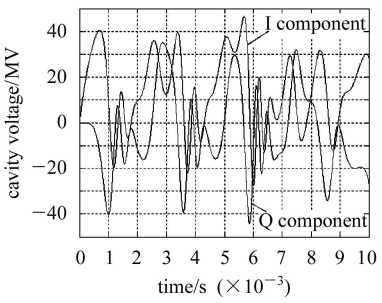

Fig. 4. Step response of the cavity simulator.

3 Cavity controller design

3.1 Demodulation of the cavity signal

The cavity controller receives the IF signal from the cavity to be controlled. The 10MHz IF signal is sampled by a 14bit ADC at the frequency of 40MHz. To get the base band I/Q components of the IF signal, the samples are stored in the sequence of "I, −Q, −I, Q", which is shown in Fig. 5.

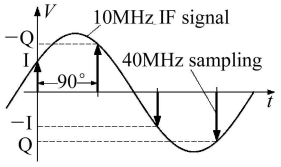

Fig. 5. Principle of the IF signal demodulation.

3.2 Vector sum generation

The cavity controller will control more than one cavity. In the case of Fig. 1, at most eight cavities can be controlled by one single cavity controller. When the beam is accelerated by these cavities, the final effect is decided by the vector sum of the cavity voltage. So, the vector sum of all the cavities is chosen to be the parameter to be controlled.

The loop phase of each cavity is quite different because of the different phase length of each RF channel. Beam is used to calibrate the loop phase of each cavity[5]. Then, the base band RF vector of each cavity is rotated to the same reference phase defined by the set point of the vector sum. Vector rotation for one cavity is performed by the formula below

$$\begin{bmatrix} V_{\mathrm{r}}' \\ V_{\mathrm{i}}' \end{bmatrix} = \begin{bmatrix} g\cos\theta & -g\sin\theta \\ g\sin\theta & g\cos\theta \end{bmatrix} \begin{bmatrix} V_{\mathrm{r}} \\ V_{\mathrm{i}} \end{bmatrix}, \qquad (3)$$

Where V_{r}, V_{i} are the real and image part of the cavity voltage before rotation, g is the loop gain and θ is the loop phase of the cavity.

After calibrating the loop phase, the vector sum is generated by adding together the real and image part of all the cavities.

3.3 Implementing the cavity controller

PI (proportional and integral) feedback control is adopted for the digital LLRF system, and feed forward control is adopted to compensate the repetition error from pulse to pulse. The System Generator program for the cavity controller is shown in Fig. 6.

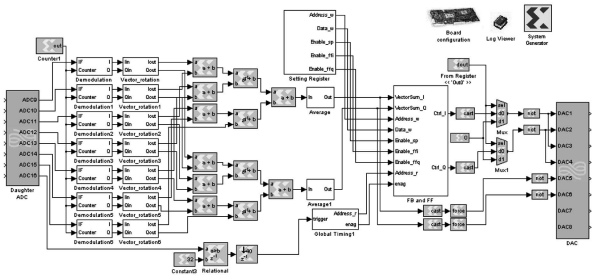

Fig. 6. FPGA program for the cavity controller.

A VHS-DAC board form the company of LYRTECH is used to implement the cavity controller. On the FPGA board, the eight ADCs are used to sample the IF signals form eight cavities or cavity simulators. Two of the DACs are used to generate the cavity control signals, which can be used to change the RF phase and amplitude feeding into the cavities. In the case of Fig. 1, the cavity control signals are fed directly to the input ADCs of the cavity simulator.

4 System test

The cavity simulator and the cavity controller are connected according to Fig. 1. In the test bellow, four cavities are controlled by the cavity controller. The vector sum of the four cavities under control is shown in Fig. 7. The cavity vector is translated into phase and amplitude, Fig. 8 shows the amplitude and phase error during the flat top of RF pulse.

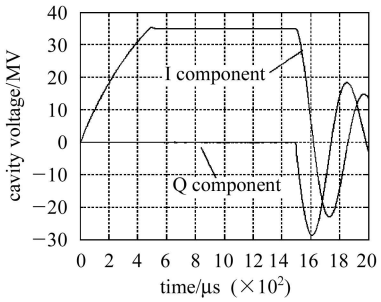

Fig. 7. Vector sum of the four cavities.

From Fig. 8 we can see that the amplitude error is less than ±0.3% (peak to peak), and the phase error is less than ±0.3° (peak to peak), which can meet the requirement of the STF LLRF system.

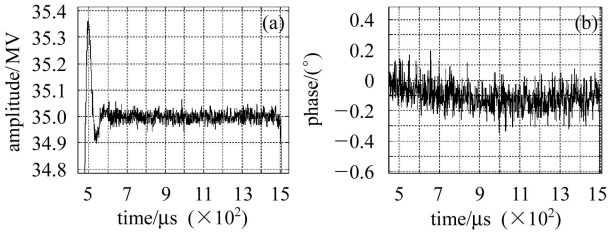

Fig. 8. Amplitude error (a) and phase error (b) during the flat top.

5 Summary

For the project of STF, the digital LLRF system is designed to provide high precise RF control. FPGA is used to implement the PI feedback and feed forward algorithms, which is suitable for fast digital signal processing so that it is possible to decrease the feedback loop delay. To test the performance of the LLRF system, a real time cavity simulator is designed and implemented in FPGA. Closed loop test of the system shows that both the cavity simulator and the cavity controller work well.

At KEK, the cavity simulator will be used to test the commercial LLRF system for STF, and the cavity controller will act as a backup of the commercial cavity controller.

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STF 数字微波低电平系统研究*

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摘要　STF 是KEK 为国际直线对撞机(ILC)建立的试验装置. 在STF 中, 数字微波低电平系统用于控制超导腔的RF 相位和幅度. 在没有实际腔运行的情况下, 设计了一个基于FPGA 技术的实时超导腔模拟器, 用于测试微波低电平系统的硬件和算法. 超导腔的数字控制器用FPGA 实现, 其中采用了PI 反馈控制和前馈控制算法. 测试表明, 超导腔模拟器和控制器都工作良好, 可用于STF 微波低电平系统的进一步开发.

关键词　数字微波低电平　FPGA　腔模拟器　STF

2006 – 11 – 10 收稿,　2007 – 01 – 04 收修改稿

∗ 国家自然科学基金(10575115)和JSPS 资助

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