Development of a prototype of the ME readout electronics onboard the HXMT satellite*

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Abstract A prototype of the ME readout electronics onboard the Hard X-ray Modulate Telescope (HXMT) satellite is developed. Application Specific Integrated Chip (ASIC) is used to construct the front end electronics due to a large number of detectors. Field Programmable Gate Array (FPGA) is connected to the ASIC as a state machine controller and data FIFO in the DAQ system. A USB board is designed to communicate between the DAQ system and the computer. The design goals and features, the operation of the system and the preliminary performance of the prototype are described. The testing results show that the design goals of the prototype system have been achieved.

Key words HXMT, ME, DAQ, ASIC, FPGA

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1 Introduction

The Hard X-ray Modulation Telescope (HXMT) is an X-ray satellite devoted to a sensitive broad band (1–250 keV) survey and pointed observations [1–3]. In order to cover this broad energy band, HXMT contains three kinds of scientific instruments: the High Energy X-ray Telescope (HE, NaI/CsI), the Medium Energy X-ray Telescope (ME, Si-PIN), and the Low Energy X-ray Telescope (LE, SCD). Apparently, ME acts as a bridge between HE and LE so as to constitute the detection capability of HXMT in the medium energy band. Since HE is only sensitive above 20 keV and the detection efficiency of LE decreases significantly above 8 keV, ME should have a low energy threshold well below 8 keV and a high energy threshold far above 20 keV. The detailed requirements to ME are listed in Table 1.

We use Si-PIN as the detectors of ME. Since the increase of Si-PIN pixel size brings higher noise, ME is made up of about 1000 small Si-PIN pixels, and so about 1000 channels of readout electronics are needed. However, the power supply, weight, and volume budgets are limited onboard the satellite. It is impossible to construct the front end electronics with separated components. Therefore, we use the Application Specific Integrated Circuit (ASIC) technology to solve this difficulty.

Table 1. The performance requirement of ME.

collection area	1000 cm^2
energy range	5 – 30 keV (−20 ℃)
energy resolution	3 keV@20 keV (−20 ℃)
timing resolution	1 ms

2 Overview of the RENA-3 chip

The ASIC we used for ME is RENA-3, a commercial product of NOVA R&D Inc. This is a 36-channel, mixed signal, low-noise, programmable ASIC for front end electronics of solid state detectors. A simplified block diagram for one channel of the RENA-3 ASIC is given in Fig. 1. Each channel consists of the charge

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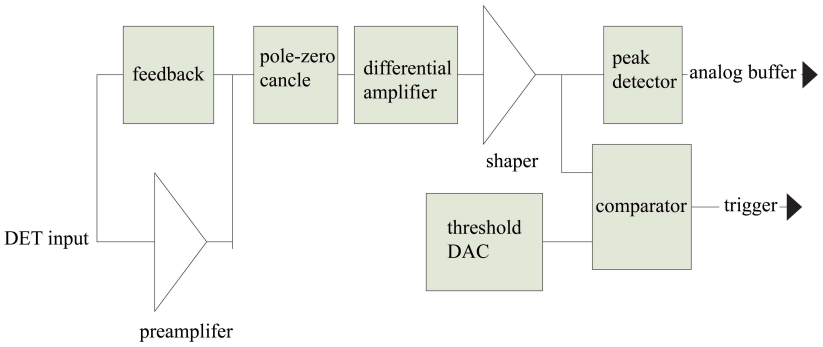

Fig. 1. A simplified block diagram for one channel of the RENA-3 ASIC.

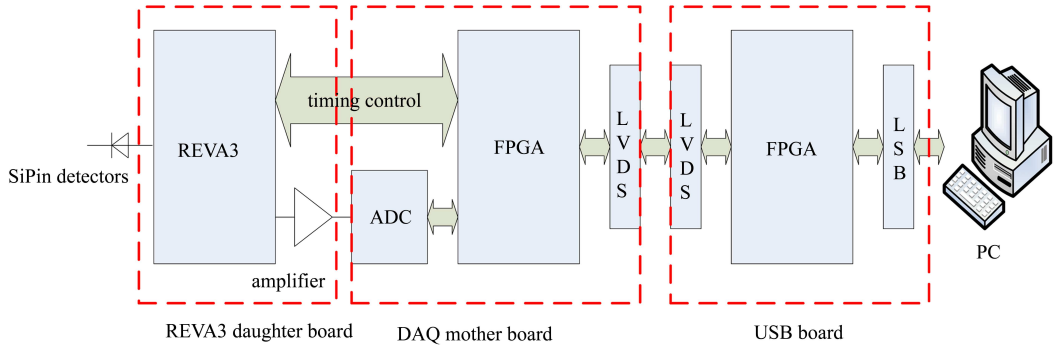

Fig. 2. The block diagram of the whole ME prototype.

sensitive preamplifier, pole-zero cancel, differential amplifier, shaper, peak detector, and trigger circuit [4]. The shaper's shaping time is selectable, allowing RENA-3 to be used for many different kinds of solid state detectors. The adjustment of the detection threshold is achieved by using a DAC at each comparator that outputs the trigger signal. The power consumption of each channel is less than 6mW. Using RENA-3 to construct the ME frontend electronics will largely reduce the system power consumption.

3 Technical design of the prototype of the ME readout electronics

3.1 Structures

The function of the prototype of the ME readout electronics is to readout the signal from detectors, acquire and timestamp the event data, and then transfer them to a computer. The block diagram of the whole system is shown in Fig. 2, where three different parts can be distinguished: the RENA-3 daughter board, the DAQ mother board, and the USB board. Field Programmable Gate Array (FPGA) is used on the DAQ mother board as a state machine controller for the RENA-3 chip; it is also a data FIFO that stores the event data. The LVDS signal, which is very suitable for long distance and high speed data transfer, is used to send the event data to the USB board that is connected with the PC. Software is developed on the PC to control and test the electronics.

3.2 The RENA-3 daughter board

The block diagram of the RENA-3 daughter board is shown in Fig. 3. A RENA-3 chip and an AD8042

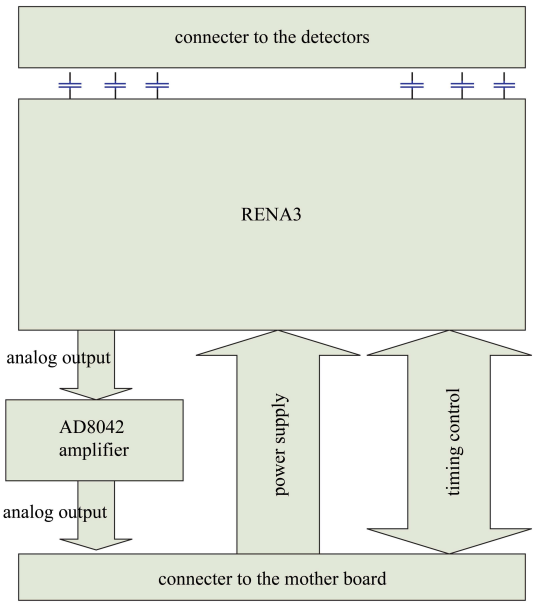

Fig. 3. A block diagram of the RENA-3 daughter board.

amplifier chip that drives the analog output of the RENA-3 chip are mounted on the board. The timing control signal, the analog output, and the power supply of RENA-3 are all connected to the DAQ board through a 20×2 pins connecter.

3.3 DAQ Mother board

3.3.1 Overview

The structures of the DAQ mother board are shown in Fig. 4. All of the power supply regulator chips are mounted on the mother board in order to reduce the noise coupling to the RENA-3 chip. The very low noise regulator chip LT1763 (20 μVrms from 10 Hz to 100 kHz) is used to generate the very low noise 5 V and 2 V power supply to RENA-3. Since the timing control signal of the RENA-3 chip is of 5 V logic standard, while the input and output of FPGA is of 3.3 V logic standard, the bus transceiver SN74LVCC3245 is used as the voltage converter interface between the RENA-3 and the FPGA. An AD9243 chip, which is a 3 MSPS, single supply, 14-bit ADC with a truly differential input structure, is used to A/D convert the differential analog output signals of RENA-3.

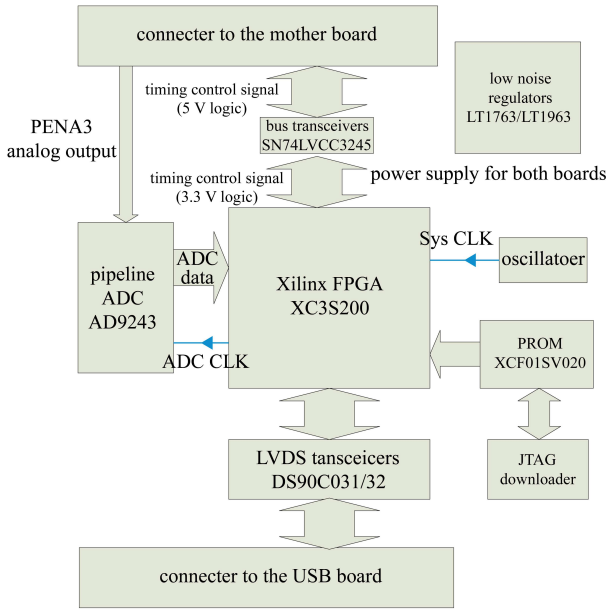

Fig. 4. A photograph and block diagram of the DAQ mother board.

3.3.2 The logic of FPGA

A Xilinx Spartan XC3S200 FPGA is used as a state machine controller for the RENA-3 chip and the ADC, which is also a data FIFO to store the scientific event data and transfer them to the USB board. The framework of the FPGA logic is shown in Fig. 5. The logic can be divided into several different modules, which will be described in the next paragraph.

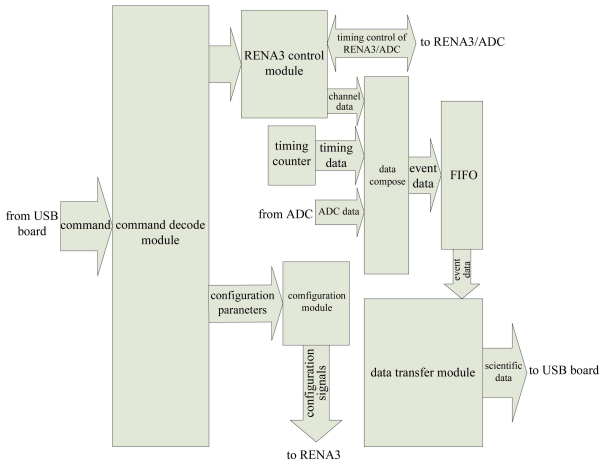

Fig. 5. A logic diagram of the FPGA on the DAQ mother board.

The working of the whole logic is realized by the cooperation of different modules. First of all, the command decode module receives the Start Configuration Command from the USB board and the configuration module start to configure the RENA-3 chip. After that, the Mode Select and Start Command will be received, and the control module will start to timing control the RENA-3 chip and the ADC to work at the selected mode. The time data (generated by a timing counter), the channel data and the energy data (digital value of the ADC output) will be acquired through working, and the data composing module combines them into a single event. At last, the FIFO module will store the event data, which need to be readout, parallel to serial convert, and then transfer to the USB board through the LVDS interface by the data transfer module.

3.3.3 The control of RENA-3

The timing control of the RENA-3 peak detector mode includes four states of operation [5]. The first state is the resetting of the Analog Signal Paths and Hit Register Flags. This is accomplished by setting the CLS input high. After the chip is reset, the channels wait for trigger events, which is the second state. In the third state, after the TS output signal is high, which means at least one channel is hit, the Hit Register Flags need to be read out and written back in using the SHRCLK, SOUT and SIN signals. In the last state, which is entered by setting READ input high, each triggered channel's peak hold signals are sequentially output to the AOUTP/N by clocking the TCLK input signal. Fig. 6 shows the timing control diagram of RENA-3. The readout of a single event

will take less then 1 ms, which is the system dead time.

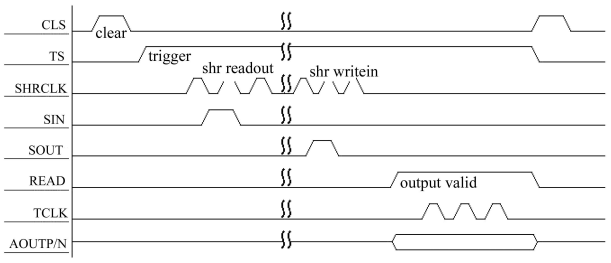

Fig. 6. The timing control of RENA-3.

There is another test mode called follower mode for RENA-3 to check the analog section of the chip. In the follower mode, the peak hold circuit of RENA-3 is disabled and the shaped output signal of the selected channel appears at the output of the chip.

3.3.4 The configuration of RENA-3

The configuration of RENA-3 is done by using three signals CS, CShift, Cin, and a 41-bit shift register. The configuration of the RENA-3 will always be performed by loading a 41-bit word of data into the serial shift register, in which the first 6 bits represent the channel address and the rest bits represent parameters. The configuration parameters can be easily set by the software on PC, then transferred to the FPGA on the DAQ board, which executes the configuration timing control of RENA-3.

3.4 USB board

The structure of the USB board is shown in Fig. 7. It is mounted with a Xilinx XC3S200 FPGA and a USB chip CY7C68001. The USB board is the interface between the DAQ and the PC, which transfers the command data and the event data. The communication between the DAQ and the USB board is described in the next paragraph.

3.5 Communication between the DAQ and the USB board

The communication between the DAQ system and the USB board is realized by 4 pairs of LVDS signals: CLK, EN, DIN (from USB board to DAQ) and DOUT (from the DAQ to the USB board). The communication is started while EN goes low and ended while EN goes high. DIN is used to transfer the event data package from DAQ to USB board, available on the rising edge of CLK. DOUT is used to transfer the command and configuration parameter data from the USB board to DAQ, available on the falling edge of CLK.

Every event contains 32 bits of data, 10 bits for timing information, 8 bits for channel number, and 14 bits for energy (ADC digital output). The event data package contains 127 event data (4 bytes each) and 4 bytes check sum, 512 bytes totally. The command data contain 8 bytes, 1 byte for the command head, 6 bytes for the command parameters, and the last byte for check sum.

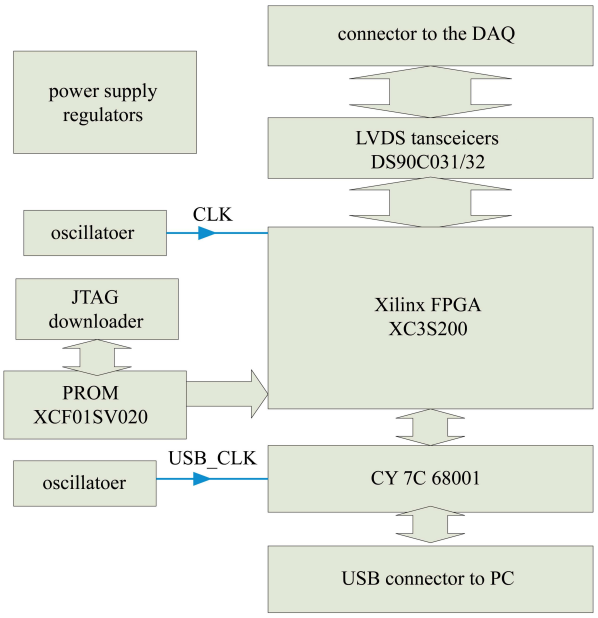

Fig. 7. A block diagram of the USB board.

3.6 Software on PC

The software on PC is developed to set the configuration parameters of RENA-3 and to control the working mode of the DAQ system. As shown in Fig. 8 during the test, the spectrum of each channel can be lively displayed through the software interface.

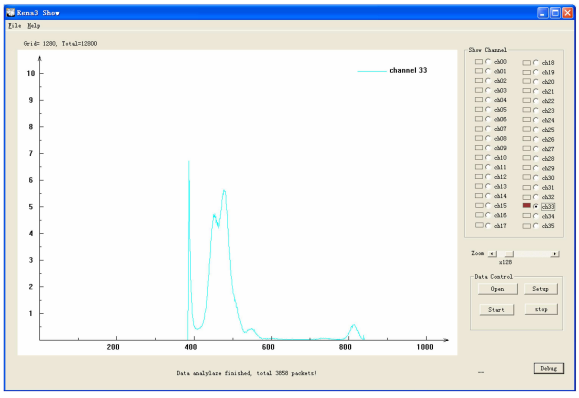

Fig. 8. Screen shot picture of the software interface.

4 Test of the prototype of the ME readout electronics

4.1 Test on one channel of the readout system

In order to test the performance of a single channel of the readout system, we measured the X-ray spectrum of ^{241}Am using a Si-PIN with a first stage FET mounted on a PCB in conjunction with the RENA-3 chip through a 50 pf capacitor. The thickness and area of the Si-PIN detector are 1 mm and 10 mm×10 mm respectively. We first used an energy range of about 0–35 keV and the acquired spectrum is presented on the left panel of Fig. 9. It shows that

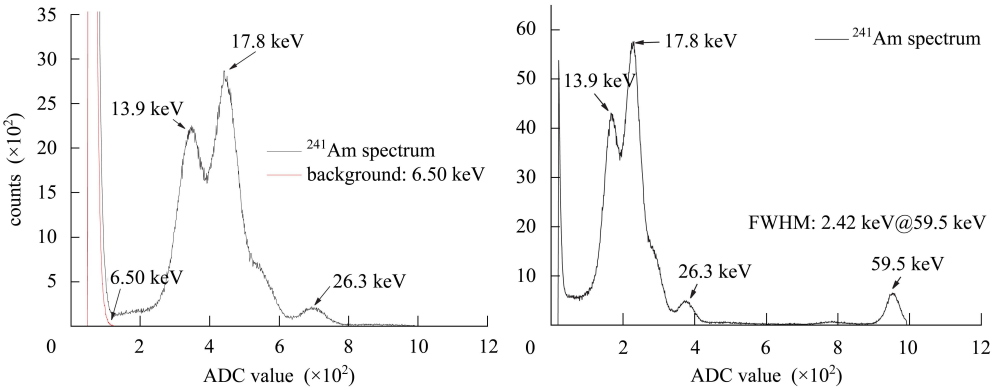

Fig. 9. The ^{241}Am spectra measured by a single Si-PIN detector at room temperature. The area and thickness of the detector are 10 mm × 10 mm and 1 mm respectively.

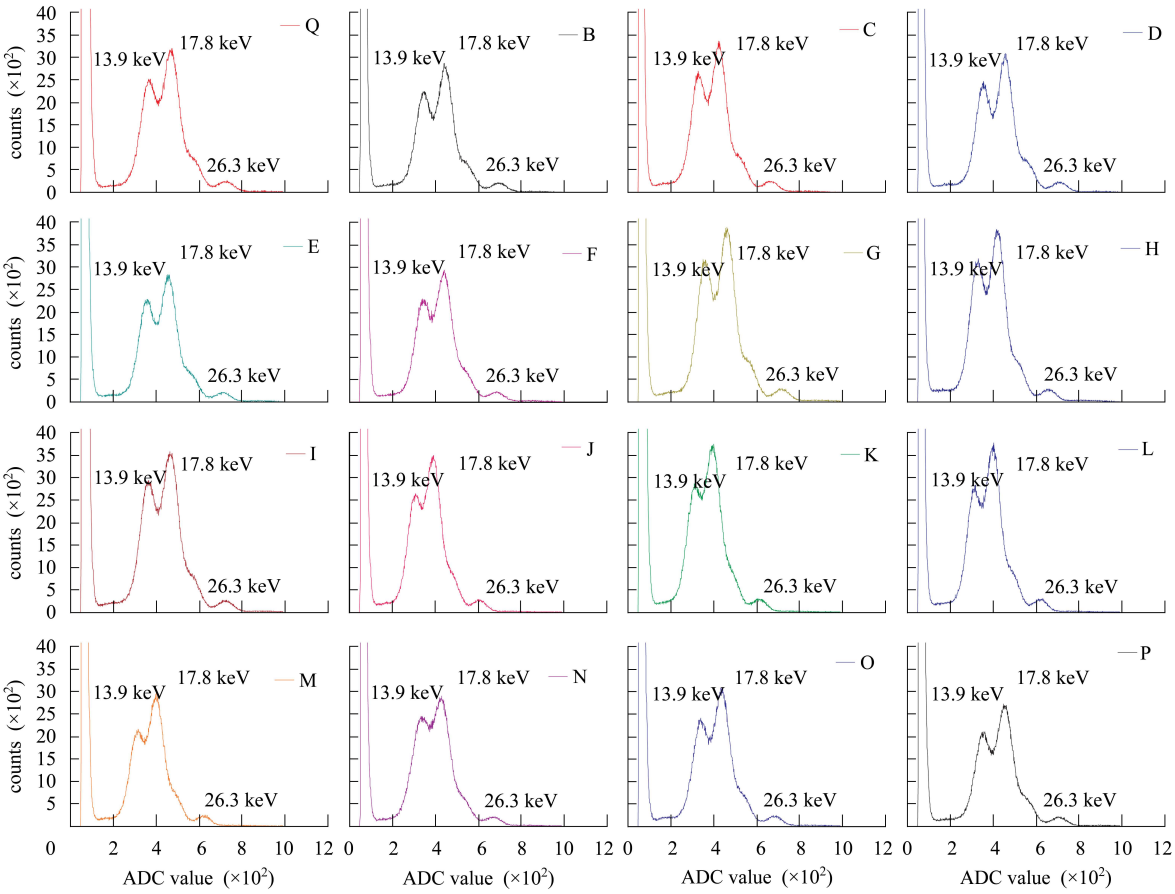

Fig. 10. 16 ^{241}Am spectra measured simultaneously by the prototype of the ME readout system at room temperature.

the system background is below 6.5 keV. However, the three X-ray lines of ^{241}Am in this energy range are so close to each other that the spectral resolution could not be explicitly displayed. We then changed the amplitude of RENA-3 to widen the test energy range to about 0–65 keV, and now the 59.5 keV line of ^{241}Am is detected, which is isolated from the other lines as shown on the right panel of Fig. 9. From this 59.5 keV line the spectral resolution of the system could be reliably obtained, which is 2.42 keV@59.5 keV. The above measurements were done at room temperatures.

4.2 Test on the multi-channels readout system

Now we make 4×4 pixels of Si-Pin detectors and their respective first stage FETs on a single module. Each pixel is 10 mm × 10 mm large and 1 mm thick. The outputs of the 16 detectors are connected to the inputs of one RENA-3 chip through 50 pF capacitors. The 16 channels of RENA-3 work simultaneously, and 16 spectra of ^{241}AM are acquired. The measured backgrounds of all pixels are below 7 keV. Apparently, the performance of the multi-channel readout system is as good as a single channel. Fig. 10 shows all the 16 spectra, which were measured at room temperature.

4.3 Test at low temperature

In order to test the performance of the system at low temperature, we cooled the detector and the FETs to −5 ℃ and the acquired spectrum of ^{241}Am is presented in Fig. 11. It shows that the system background is below 5 keV and the spectral resolution is 2.08 keV@59.5 keV, which are much better than at room temperature. It is expected that the performance will be even better at the ME's in-orbit working temperatures (−40 to −20 ℃)

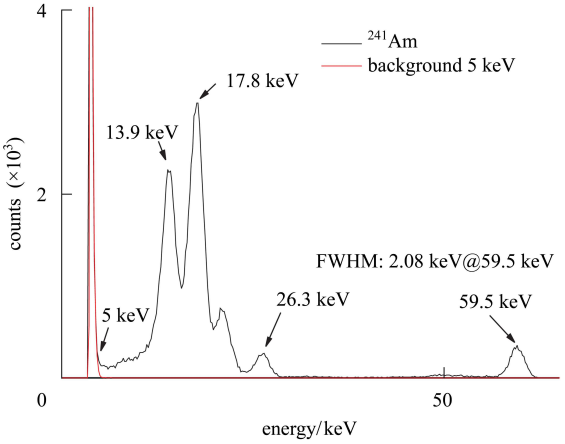

Fig. 11. The ^{241}Am spectrum obtained by a single Si-PIN detector with an area of 10 mm × 10 mm and thickness of 1 mm. The measurement was done at −5 ℃.

5 Summary

The prototype of the ME readout electronics has gone through the design and R&D stage. The main results of the tests show that, at room temperature, the background of the system is below 7 keV, and the energy resolution is better than 2.5 keV@59.5 keV. The performance of the system can be improved when working at a lower temperature. The background of the system is lower than 5 keV and the energy resolution is 2.08 keV@59.5 keV at −5 ℃. The system satisfies the multi-channel readout function, and the timing resolution of the system is better than 1ms. The requirements of the ME system will be met through copying this prototype.

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