High accuracy amplitude and phase measurements based on a double heterodyne architecture

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Abstract: In the digital low level RF (LLRF) system of a circular (particle) accelerator, the RF field signal is usually down converted to a fixed intermediate frequency (IF). The ratio of IF and sampling frequency determines the processing required, and differs in various LLRF systems. It is generally desirable to design a universally compatible architecture for different IFs with no change to the sampling frequency and algorithm. A new RF detection method based on a double heterodyne architecture for wide IF range has been developed, which achieves the high accuracy requirement of modern LLRF. In this paper, the relation of IF and phase error is systematically analyzed for the first time and verified by experiments. The effects of temperature drift for 16 h IF detection are inhibited by the amplitude and phase calibrations.

Key words: amplitude and phase measurements, double heterodyne architecture, wide IF, non-IQ sampling, LLRF

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1 Introduction

The low level RF (LLRF) system is an important component for the RF system of particle accelerators and typically includes three control loops: phase, amplitude, and frequency of cavity RF field [1]. The precision and stability of these loops depend on the amplitude and phase measurements of the RF signals coupling from the cavity. The new generation of accelerators requires that the cavity RF field has high accuracy and high stability, such as 0.07% and 0.24° for the International Linear Collider [2], 0.01% and 0.01° for the Europe X-ray Free Electron Laser [3].

In traditional amplitude and phase measurements that are based on heterodyne architecture, as shown in Fig. 1(a), the RF signal is down converted to a fixed intermediate frequency (IF). It is then sampled by an ADC and the IQ information is extracted by digital signal processing. However, the ratio of IF and sampling frequency determines the digital signal processing required. This differs in various LLRF systems. See Table 1 for the differences. So it is very useful to design a universally compatible architecture for different ratios of IF and sampling frequency with no change to the digital signal processing algorithm.

In this paper, an advanced heterodyne architecture, which is called a double heterodyne architecture, based on non-IQ sampling is proposed. It relaxes the range of IF input. The amplitude and phase measurements have been realized with IF from 1 to 30 MHz. The stability is 0.003° (rms) for phase and 0.012% (rms) for amplitude with IF at 1 MHz. For different IFs, we just need to change one parameter of the second heterodyne architecture, which is convenient.

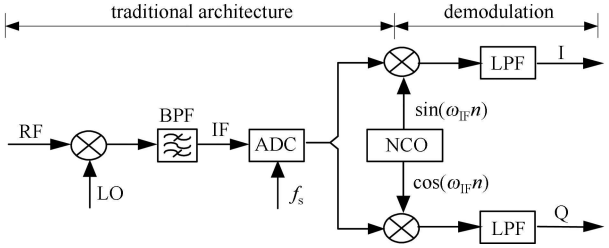

Fig. 1. Traditional IQ demodulation based on heterodyne architecture.

Table 1. Parameters of some LLRF systems based on a heterodyne architecture.

heterodyne+IF oversampling or IF sampling			
reference	Ref. [4]	Ref. [5]	Ref. [6]
IF frequency/MHz	1	3	13
sampling rate/MHz	100	122.88	62.524

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2 Double heterodyne architecture

The amplitude and phase measurements contain two stages. Firstly, in the double heterodyne architecture (Fig. 2), the RF signal is down converted to the first IF ($y_{\rm IF1}(t)$) in the analog domain. The lower sideband is extracted by a BPF. This can be expressed as

$$y_{\rm IF1}(t)=A\cos(2\pi f_{\rm IF1}t+\varphi_0), \tag{1}$$

where $f_{\rm IF1}=|f_{\rm RF}-f_{\rm LO}|$, and $f_{\rm LO}$ is the local frequency. To sample this signal, the relations $0<f_{\rm IF1}<\frac{f_{\rm s}}{2}$ should be obeyed. Here fs is the sampling frequency of the ADC.

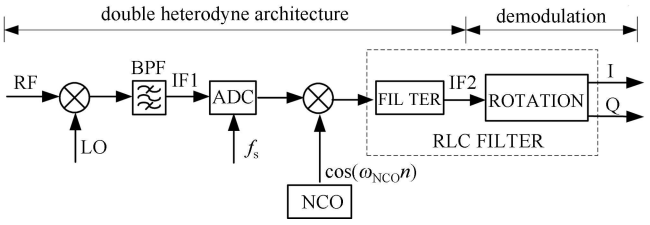

Fig. 2. A diagram of the proposed double heterodyne architecture.

The amplitude and phase can then be obtained by digital signal processing algorithm. It is implemented as follows. The $y_{\rm IF1}(t)$ is converted to the second IF in digital domain. In this progress (Fig. 2), we combine an improved Numerical Controlled Oscillator (NCO) with a narrow band IIR filter, which is called a RLC filter.

In the proposed architecture, the improved NCO and the RLC filter are critical. They are introduced in Section 3.2. The first IF sequence mixes with a digital local signal. This is generated by the improved NCO, which can generate any frequency, and is limited by the Nyquist frequency. For different IF detection, we simply need to change the output frequency of the NCO. The IF sequence and the output sequence of the NCO will then be mixed in the digital domain. The corresponding lower band signal centered about a fixed frequency ($f_{\rm RLC}$) is filtered out. This is the second IF sequence

$$y_{\rm IF2}(n)=\frac{A}{2}\cos(\omega_0 n+\varphi_0). \tag{2}$$

The analog radian frequency (Ω_0) and the digital radian frequency (ω_0) are given, respectively, by

$$\Omega_0=2\pi f_{\rm IF2},\quad \omega_0=\Omega_0 T, \tag{3}$$

where T is the sampling period, and $f_{\rm IF2}=f_{\rm RLC}$. A rotation algorithm is included in the RLC design to demodulate the IQ components. The IQ components of $y_{\rm IF2}(n)$ can be expressed as

$$I_0=\frac{A}{2}\cos(\varphi_0),\quad Q_0=\frac{A}{2}\sin(\varphi_0). \tag{4}$$

The amplitude and phase can then be calculated by the CORDIC (coordinate rotation digital computer) algorithm.

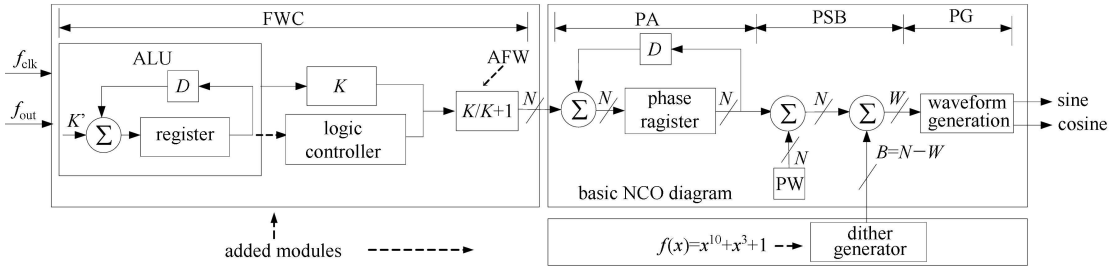

Fig. 3. A diagram of the proposed double heterodyne architecture.

3 Core algorithms

3.1 Improved NCO

For a traditional NCO, the output frequency is

$$f_{\rm out}/f_{\rm clk}=K/2^N,\quad K\in Z^+. \tag{5}$$

An improved design of NCO, as shown in Fig. 3, is presented in this paper. The output frequency and the clock frequency are at any proportion

$$f_{\rm out}/f_{\rm clk}=Q/P,\quad Q\in Z^+,\quad P\in Z^+. \tag{6}$$

The improved NCO adds a frequency word controller (FWC), which is similar to a fractional N divider [7], to calculate the frequency word (FW) per clock cycle. In a traditional NCO, phase truncation error and amplitude quantization error will cause spurious signals. The improved NCO addresses this problem by injecting random noise in the phase summing block. In the second heterodyne architecture, it is processed by a digital local oscillator.

3.2 The band-pass RLC filter

Digital filters are important for extracting IQ information (Fig.1). At present, digital low pass-band filters,

such as Cascaded Integrator-Comb (CIC) filters and FIR filters, are widely used. However, a CIC filter has a high pass-band droop and a low attenuation in the folding bands (bands around the comb zeros) [8]. Meanwhile a narrow band low-pass FIR filter requires a high order.

In this paper, a narrow IIR filter is adopted to extract and demodulate the second IF signal $y_{\rm IF2}(n)$. This filter is based on a series RLC resonant circuit [9]. Its impulse response function of the first-order RLC filter is

$$h(n)=\mathrm{e}^{-\alpha Tn+\mathrm{j}\omega_0 n}. \quad (7)$$

Here ω_0 is the digital radian frequency and T is the sampling period, as mentioned above. Parameter α and quality factor Q satisfy $\alpha=\omega_0/2QT$, $Q=1/R\sqrt{(L/C)}$. The bandwidth of one single-order RLC filter is $B_1=2\alpha T=\omega_0/Q$. A k-stage RLC filter is cascaded by a multiple single-order RLC filter, whose bandwidth is $B_k=B_1\cdot\sqrt{2^{1/k}-1}$. Compared with traditional narrow band filters, it has a simpler structure, less delay, and higher precision.

4 The system error analysis

In practical measurement, the amplitude and phase errors are mainly affected by three factors, as follows:

1) RF source and RF devices;

2) The performance of high-speed ADC; and,

3) Digital signal processing methods.

For long time test, temperature drift should be considered.

Table 2. Main parameters of the detection platform.

parameter	index
sampling rate	150 Msps
IF signal frequency	1–30 MHz
bandwidth	100 kHz
clock Jitter for FPGA	1.36 ps (rms)
clock Jitter for ADC	10.7 ps (rms)
width of ADC	14-bit
DNL of ADC	±0.4 LSBs
effective input noise	2.72 LSBs

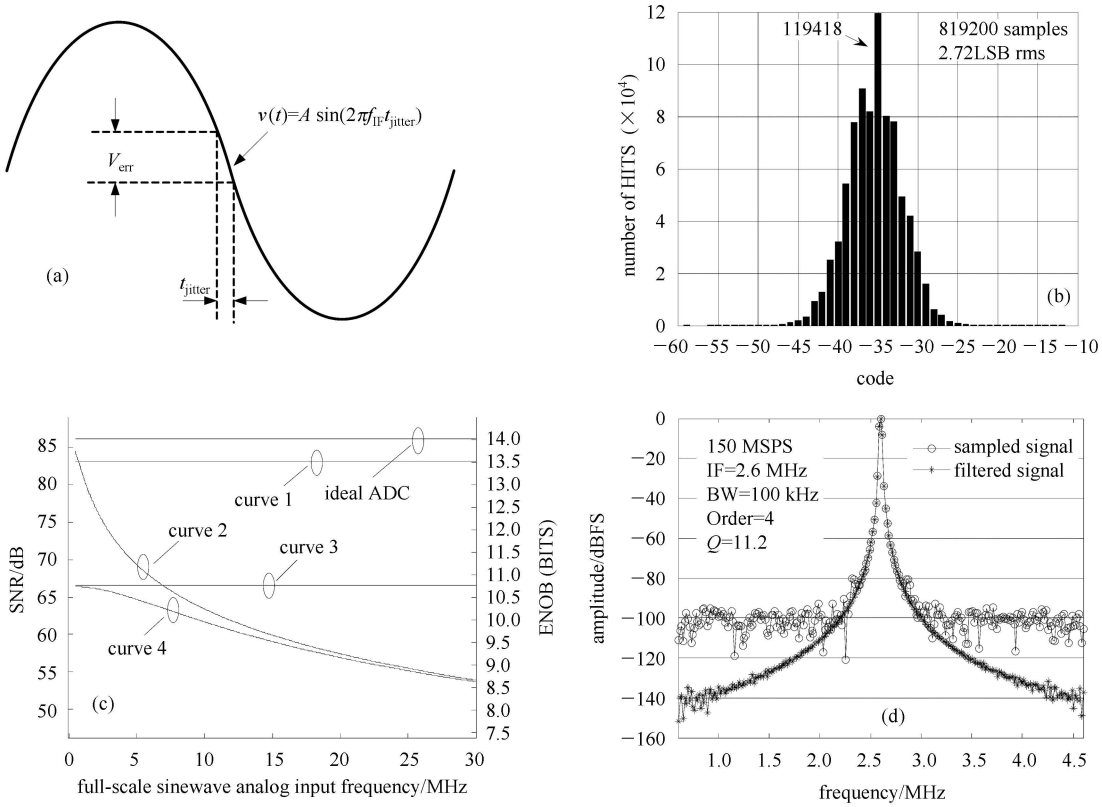

Fig. 4. The error analysis based on jitter, effective input noise, and DSP method. (a) The effect of clock jitter on the sampled signal. (b) The ADC grounded input histogram. See text for details. (c) Simulation of ADC performance with different parameter values (Ideal ADC: only quantization noise included; curve 1: only quantization noise and DNL equal to ±0.4 LSB considered; curve 2: only quantization noise and clock jitter equal to 10.7 ps included; curve 3: only quantization and input effective noise equal to 2.72 LSBs included; curve 4: our system with quantization noise, DNL, clock jitter and input effective noise and special values in Table 2). (d) Spectrum of the oversampled signal by ADC and the output signal of the RLC filter.

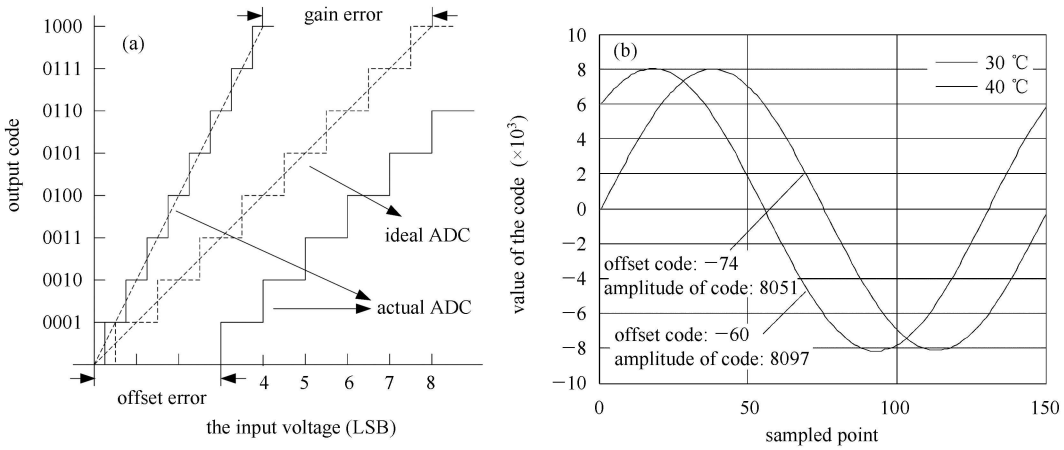

Fig. 5. Error analysis due to temperature variations and corresponding pointed solution. (a) Gain and offset errors. (b) Test of gain and offset error. A signal of 1 MHz has been sampled by AD9254 with 14-bit 150 Msps under different temperatures and recorded by a SignalTap Ⅱ Logic Analyzer.

In the LLRF system, the SNR of the IF signal depends on the RF source and RF devices, including amplification, down conversion, and the analog filtering process. The noise in the measured signal will be converted into digital noise.

The performance of an ADC directly affects the accuracy of the system. Eq. (8) shows the ADC SNR in terms of sampling clock and aperture jitter, differential nonlinearity (DNL), effective input noise, and the number of bits of resolution [10]

$$\mathrm{SNR} = -20\log_{10}\left[(2\pi f_{\mathrm{a}}t_{\mathrm{jitter}})^2+\frac{2}{3}\left(\frac{1+\varepsilon}{2^N}\right)^2 + \left(\frac{2\sqrt{2}V_{N\text{-rms}}}{2^N}\right)^2\right]^{\frac{1}{2}}, \quad (8)$$

where f_{a} is the analogy input frequency of the full-scale input sinewave; t_{jitter} is the combined rms jitter of the internal ADC and eternal clock; ε is the average DNL of the ADC; N is the number of bits in the ADC; and, $V_{\mathrm{noise\text{-}rms}}$ is the effective input noise of the ADC. Fig. 4(a) illustrates how the aperture jitter introduces errors into the sampled signal. The maximum voltage error is [11]

$$V_{\mathrm{err}}=2\pi f_{\mathrm{IF}}t_{\mathrm{jitter}}A. \quad (9)$$

It can be manifested in phase error

$$\phi_{\mathrm{err}}=360^\circ t_{\mathrm{jitter}}f_{\mathrm{IF}}, \quad (10)$$

where f_{IF} is the IF frequency. The performance of the high speed ADC is sensitive to aperture jitter, including the ADC aperture jitter and especially the clock jitter. Eq. (10) says that there is a positive correlation between phase error and IF, which is certified in our experiments.

The primary factors in our test system, which are mentioned in Eq. (8), have been tested and analyzed. They are summarized in Table 2. As shown in Fig. 4(b), the effective input rms noise is 2.72 LSBs [12]. According to Eq. (8), the curves of IF versus SNR or ENOB are plotted in Fig. 4(c). Curve 2 and Curve 3 intersect at IF approximately equal to 7 MHz. This means that the SNR of our system is mainly restricted by the effective input noise and aperture jitter. The system is dominated by aperture jitter with IF 7–30 MHz. Oversampling technology and the digital RLC filter obviously help enhance the SNR of the IF signal, as illustrated in Fig. 4(d).

The performance of the ADC can be affected by temperature drift, such as gain error and offset error. As shown in Fig. 5(a), the gain error is multiplied by the measured value. The offset error is added to the measured value. As a result of temperature variation, the offset code and amplitude code have changed, which is shown in Fig. 5(b). These variations can cause slow amplitude and phase drifts, which are confirmed in Section 5.

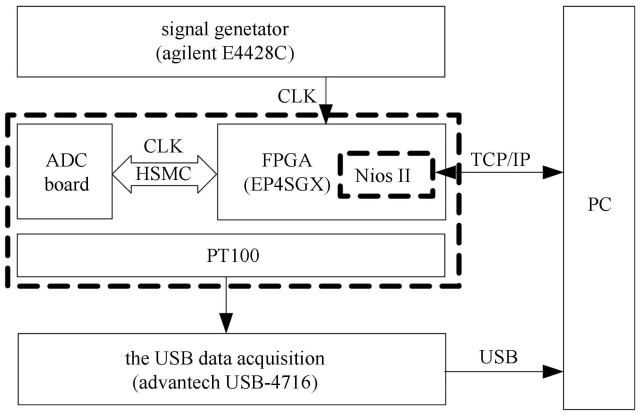

Fig. 6. Diagram of the experiment system.

5 Experiment and results

Figure 6 shows a diagram of the experiment system. The main parameters of the IF detection platform are shown in Table 2. In the LLRF system, we pay more attention to the relative accuracy than absolute accuracy. The phase of the test signal is subtracted from the phase of the reference signal, which gives the calibrated phase. We divide the amplitude of the test signal by the amplitude of the reference signal, which gives the calibrated

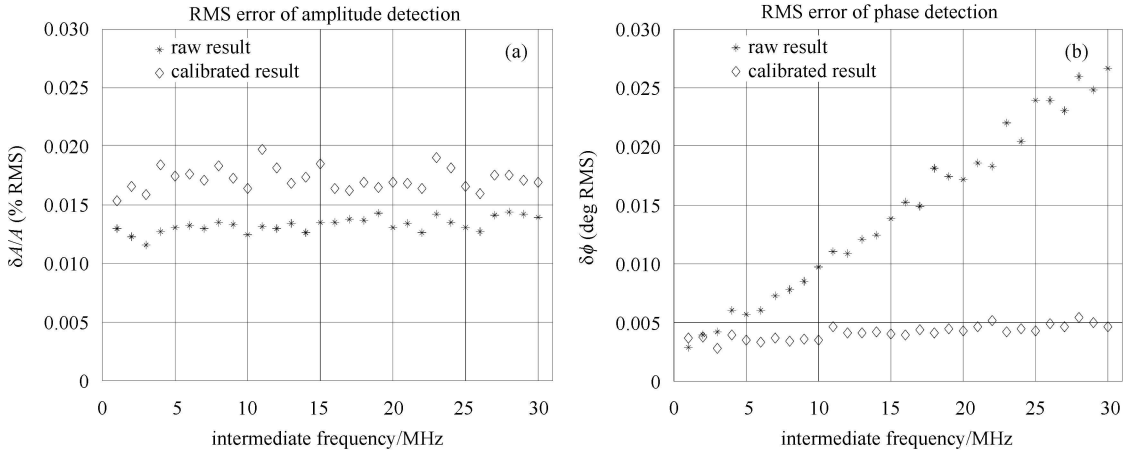

Fig. 7. The RMS errors of amplitude and phase versus different IFs before and after calibration.

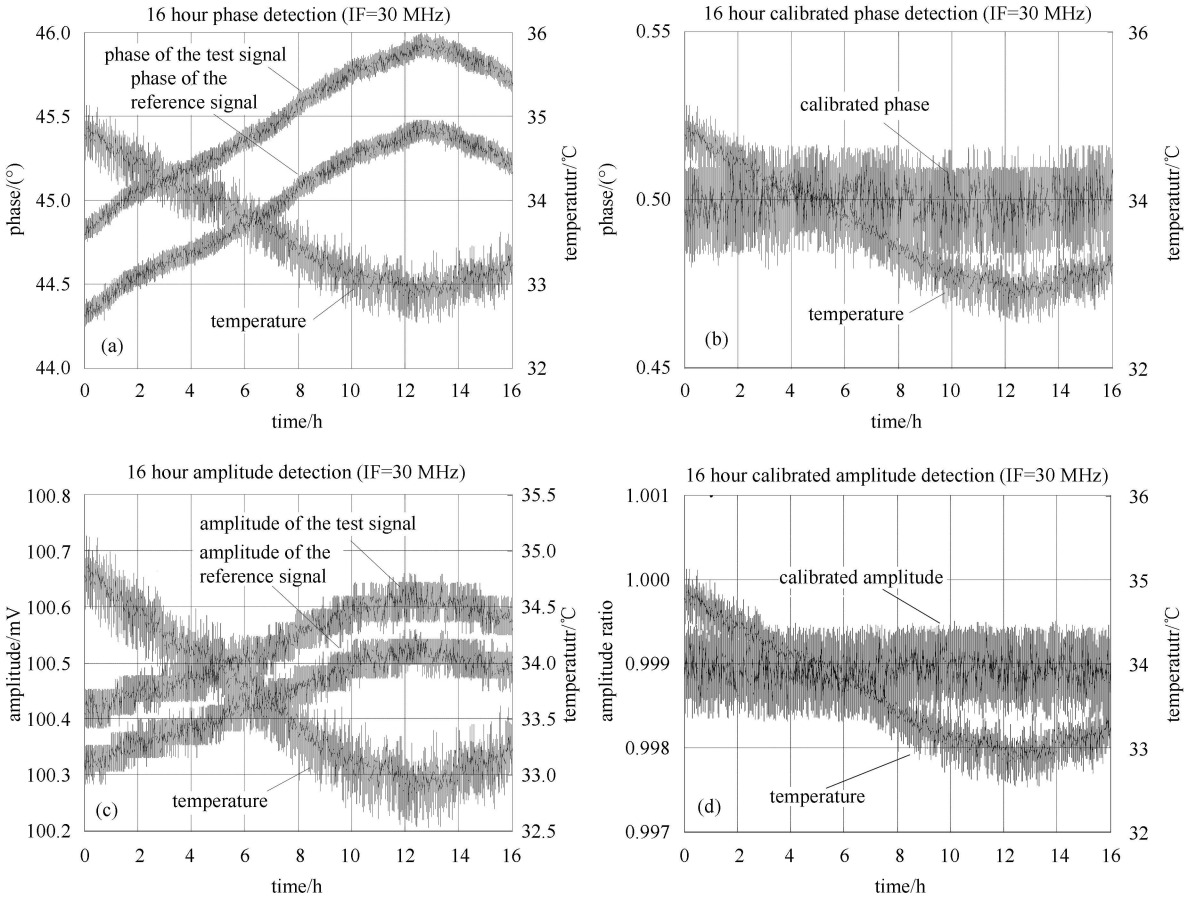

Fig. 8. Amplitude and phase detection of 30 MHz signal for 16 hours. (a) Phase detection before calibration. (b) Phase detection after calibration. (c) Amplitude detection before calibration. (d) Amplitude detection after calibration.

Table 3. Comparisons of different IFs for 3 mins.

IF signal frequency/MHz	1(raw result)	1(calibrated result)	30(raw result)	30(calibrated result)
amplitude error(Max.)	$<\pm0.033\%$	$<\pm0.043\%$	$<\pm0.035\%$	$<\pm0.048\%$
amplitude error(RMS)	$<\pm0.012\%$	$<\pm0.016\%$	$<\pm0.013\%$	$<\pm0.018\%$
phase error(Max.)	0.008°	0.009°	0.070°	0.013°
phase error(RMS)	0.003°	0.003°	0.027°	0.005°

amplitude. We have measured different IF signals (1–30 MHz) based on the double architecture. The detection accuracy levels of IF at 1 MHz and 30 MHz are summarized in Table 3. The results have reached the state-of-the-art modern LLRF.

The effect of IF is verified: although IF has less impact on the amplitude error (Fig. 7(a)), it is proportional to the phase error (Fig. 7(b)). The phase calibration can minimize the effect of IF on phase error, while amplitude calibration provides no significant improvement.

Figure 8 shows the measurement results of amplitude and phase for 16 hours. Both amplitude and phase drift to the opposite direction of temperature. The calibrations of amplitude and phase could remove the effects of temperature drift. As shown in Fig. 8(c), the amplitude before calibration decreases with the increase of temperature, which is caused by gain drift. This coincides with Fig. 5(b).

6 Conclusion

This paper presents a double heterodyne architecture. Compared with the traditional design, our architecture can be used with a wide range of IFs. Based on this architecture, amplitude and phase detections with IF from 1 to 30 MHz have been realized. The stability is 0.003° (rms) for phase and 0.012% (rms) for amplitude with IF at 1 MHz. The results have reached the demands of state-of-the-art LLRF system. Our analysis and simulation of system errors are presented. In this paper, the experiments show that phase error is proportional to the input IF, while the amplitude error is not. The phase and amplitude drift due to temperature variations can be inhibited by calibration. In our future plans, this architecture will be used to achieve high accuracy detection in the LLRF system of BEPC Ⅱ.

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