Onboard calibration circuit for the DAMPE BGO calorimeter front-end electronics*

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Abstract: DAMPE (DArk Matter Particle Explorer) is a scientific satellite which is mainly aimed at indirectly searching for dark matter in space. One critical sub-detector of the DAMPE payload is the BGO (bismuth germanium oxide) calorimeter, which contains 1848 PMT (photomultiplier tube) dynodes and 16 FEE (Front-End Electronics) boards. VA160 and VATA160, two 32-channel low power ASICs (Application Specific Integrated Circuits), are adopted as the key components on the FEEs to perform charge measurement for the PMT signals. In order to monitor the parameter drift which may be caused by temperature variation, aging, or other environmental factors, an onboard calibration circuit is designed for the VA160 and VATA160 ASICs. It is mainly composed of a 12-bit DAC (Digital to Analog Converter), an operational amplifier and an analog switch. Test results showed that a dynamic range of 0–30 pC with a precision of 5 fC (Root Meam Square, RMS) was achieved, which covers the VA160's input range. It can be used to compensate for the temperature drift and test the trigger function of the FEEs. The calibration circuit has been implemented for the front-end electronics of the BGO Calorimeter and verified by all the environmental tests for both Qualification Model and Flight Model of DAMPE. The DAMPE satellite was launched at the end of 2015 and the calibration circuit will operate periodically in space.

Keywords: DAMPE, BGO calorimeter, front-end electronics, calibration circuit, VA160

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1 Introduction

DAMPE is a scientific satellite developed in China, and planned to operate in a low earth orbit with an altitude of 500 km for a mission period of at least 3 years. Its main scientific objective is searching for dark matter particles through obtaining the e^+/e^- and γ energy spectra in space, which are thought could provide clues for dark matter [1, 2].

As a critical sub-detector of the DAMPE payload, the BGO (bismuth germanium oxide) calorimeter is responsible for precisely measuring the energy of cosmic rays from 5 GeV to 10 TeV and distinguishing positrons/electrons and gamma rays from hadron backgrounds. It also provides trigger information for the whole DAMPE payload [3, 4].

The BGO calorimeter contains 308 BGO crystal bars and 616 photomultiplier tubes (PMTs), as shown in Fig. 1. In order to achieve a large dynamic range of up to 2×10^5 for each BGO bar, each PMT incorporates a three-dynode (2, 5, 8) pick off, which results in 1848 signal channels in total. As shown in Fig. 2, the readout electronics contains 16 FEEs (Front-End Electronics

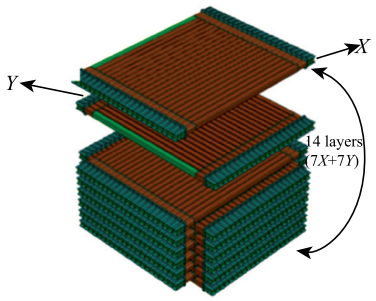

Fig. 1. (color online) Crystal bars of BGO calorimeter.

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boards) and 1848 electronics channels where each channel deals with one dynode signal. Each electronics channel is required to cover a dynamic range of 0–12 pC with a precision better than 10 fC and a nonlinearity less than 2% [5–7].

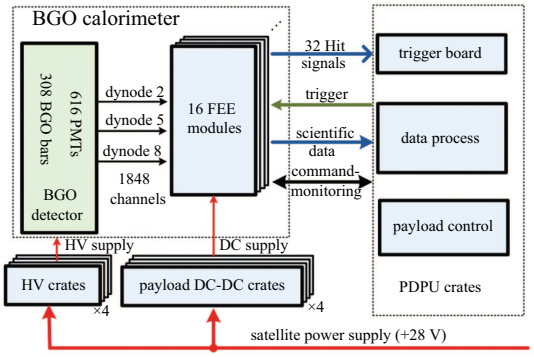

Fig. 2. (color online) The readout electronics for the BGO calorimeter.

Before launching, the BGO Calorimeter Flight Model took nearly one year to go through a series of functional tests and environmental tests, including EMC (Electromagnetic Compatibility) test, vibration test, thermal cycling test, thermal-vacuum test, 360-hour burn-in test, and a series of integration tests together with the satellite platform. During these tests, we needed to monitor the performance of every electronics channel on the FEEs. More importantly, the DAMPE satellite will operate continuously for more than 3 years in space, during which the parameters of the electronics channels may vary due to aging, temperature drift, total radiation dose, etc [8].

Therefore, onboard calibration for the front-end electronics should be carried out periodically to monitor the performance, diagnose the parameters and even further compensate the parameter distortion.

2 Architecture of the front-end electronics

According to the requirements for high integration and high mechanical strength, three types of FEE boards (FEE-A, FEE-B, FEE-C) have been designed with different dimensions. They have the same schematic except for different numbers of channels and FEE-A's additional function of generating hit signals. The FEE boards are configured with the BGO crystal layers as shown in Fig. 3. FEE-A and FEE-B contain 132 electronics channels, which are responsible for acquiring 132 dynode signals from two crystal layers. FEE-C contains 66 electronics channels, which are responsible for acquiring 66 dynode signals from only one crystal layer.

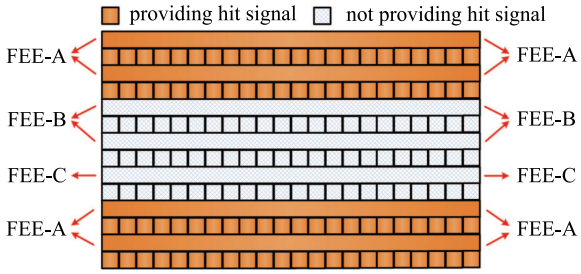

Fig. 3. (color online) Configuration for the BGO detector and FEEs. Four FEE boards are assembled with the detector on each side (16 FEEs on four sides in total). FEE-A or FEE-B takes charge of two layers while FEE-C takes charge of only one layer. In addition, FEE-A is responsible for generating hit signals.

FEE-A's schematic is shown in Fig. 4. It contains several parts: charge measurement circuit, calibration circuit, hit signal generating circuit (only in FEE-A), current and temperature monitoring circuit, power supply circuit and communication circuit between FEE and PDPU (Payload Data Process Unit). They are controlled by an Actel Flash FPGA (Field-Programmable Gate Array) [9]. Of these, the charge measurement circuit is the critical part, and is responsible for acquiring the detector's dynode signals. It is made up of 2 VA160s, 4 VATA160s, two operational amplifiers and a high-precision ADC (Analog to Digital Converter) [8].

VA160 and VATA160 ASICs are the key components on the FEEs. They are responsible for integrating and shaping the PMT signals, and sending out the

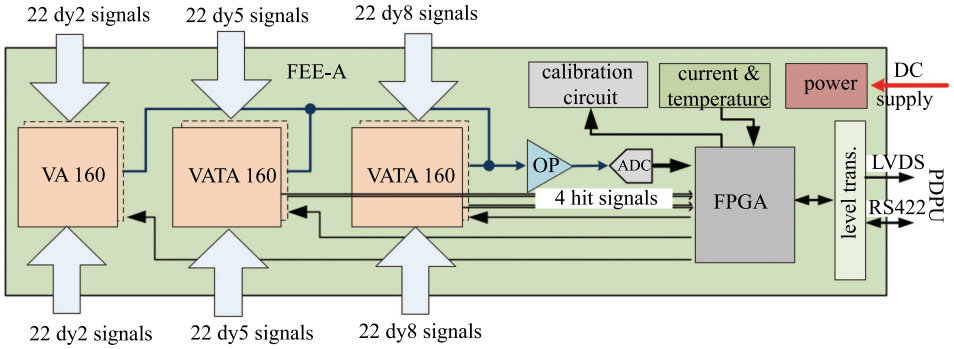

Fig. 4. (color online) The schematic of the BGO FEE.

amplitudes channel by channel. VA160 contains 32 analog channels. Each channel consists of a charge sensitive preamplifier, a first order semi-Gaussian CR-RC filter ("Slow Shaper") and a Sample-and-Hold unit. All 32 channels share a common calibration signal input (Cal), a differential output (outp/outn) and two 32-bit shift registers [10]. VATA160 can be seen as the combination of a VA160 and a TA160, where TA160 is responsible for generating hit signals. TA160 includes a fast CR-RC shaper followed by a level-sensitive discriminator for each channel. The hit signals from each channel are wire-or'ed together onto one common hit output (TA/TB) [11].

Each FEE board contains up to 132 electronics channels and up to 6 VA chips. The calibration circuit on the FEE board can be used to check all charge measurement channels and hit signal generating channels remotely. Then we can learn about the status of every electronics channel and make adjustments in real time. Furthermore, we can compensate the scientific data offline with the calibration data.

3 Design of the calibration circuit

3.1 Requirements for calibration signal

The signal waveform from the BGO detector is shown in Fig. 5. It is an exponential decay current pulse with 300 ns time constant, which is much less than the 1.8 μs peaking time of the VA160 front-end ASIC. Supposing the calibration signal is an exponential decay waveform, the time constant of the calibration signal should be much less than 1.8 μs as well.

Moreover, in order to achieve the large dynamic range for the BGO detector, a dynamic range up to 500 times should be achieved for each electronics channel. The charge of the calibration signal should cover 0–13 pC, which is the VA160's input range.

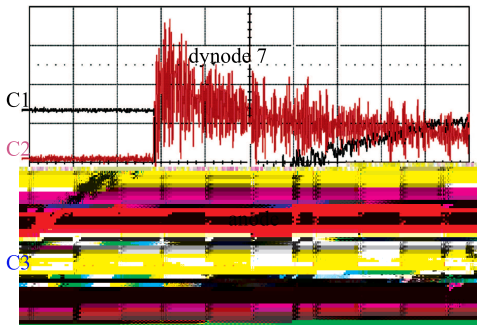

Fig. 5. (color online) The signal waveforms from one R5610a PMT coupled with a BGO crystal. The waveforms were acquired by a LeCroy 44Xi oscilloscope with 50 Ω input impedance. C1 is anode signal with 100 mV/div, C2 is dynode7 signal (similar to dynode 8 signal but with a smaller amplitude) with 5 mV/div while C3 is unconnected. The time scale is 100 ns/div [7].

3.2 Calibration signal generation

The calibration signal generation process is shown in Fig. 6. $V_{\rm dac}$ is generated by a DAC. As Eq. (1) shows, $V_{\rm ref}$ is buffered from $V_{\rm dac}$ through an operational amplifier. Two capacitors, C1 and C2, are used to filter out noise, where C1 is 33 pF and C2 is 1 nF. D1 is a diode (1N4148) used to absorb the negative overshot of $V_{\rm ref}$ caused by the analog switch switching from off to on [12].

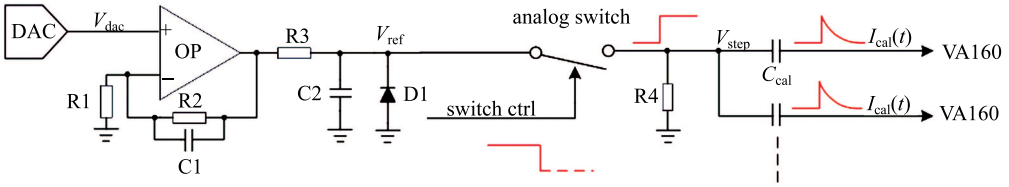

Fig. 6. (color online) Calibration signal generating circuit.

In the idle state, the analog switch is off and its output is pulled down to zero by R4. When the analog switch is on, a voltage equal to $V_{\rm ref}$ is generated at the output. Controlling the analog switch switching from off to on, we get a rising step voltage signal, $V_{\rm step}$. The waveform of $V_{\rm step}$ is shown in Fig. 7, with a rising time of about 20 ns. After $V_{\rm step}$ passes through a serial capacitor, an exponential decay current pulse, $I_{\rm cal}(t)$, is generated as the calibration signal. To obtain high-precision calibration signals, we adopt high-precision capacitors (NPO capacitor, +/−2%), $C_{\rm cal}$, and place them as close to the VA160s as possible.

$$V_{\rm ref} = \frac{\rm R1+R2}{\rm R1} \times V_{\rm dac}, \tag{1}$$

$$Q_{\rm cal} = \int_0^{+\infty} I_{\rm cal}(t){\rm d}t, \tag{2}$$

$$Q_{\rm cal} = \int_0^{+\infty} \left(\frac{1}{\rm R} V_{\rm ref} {\rm e}^{\frac{-t}{\rm RC}}\right) {\rm d}t = V_{\rm ref} C_{\rm cal}. \tag{3}$$

In Eq. (1), (2) and (3), R1 and R2 are 40 kΩ and 10 kΩ respectively and $C_{\rm cal}$ is 10 pF. The charge input into VA160, $Q_{\rm cal}$, is proportional to $V_{\rm ref}$. $V_{\rm ref}$ has a dynamic range of 0–3.0 V and accordingly $Q_{\rm cal}$ has a dynamic range of 0–30 pC, which covers the VA160's input range. The DAC has a precision of 12 bits and the FEE board has low noise, which ensures the calibration circuit has a precision of better than 5 fC.

The calibration circuit is designed with VA160's calibration function within itself. The calibration circuit serves all VA160s on a FEE board. As shown in Fig. 8, the calibration circuit mainly contains a FPGA, a DAC, an operational amplifier, an analog switch and all VA160s on a FEE board.

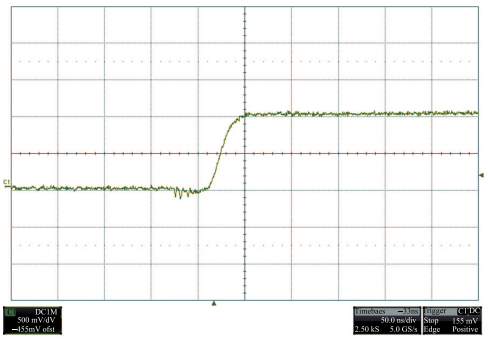

Fig. 7. (color online) Waveform of $V_{\rm step}$ before $C_{\rm cal}$. The waveform was acquired by a LeCroy 104MXs-A oscilloscope with 1 MΩ input impedance.

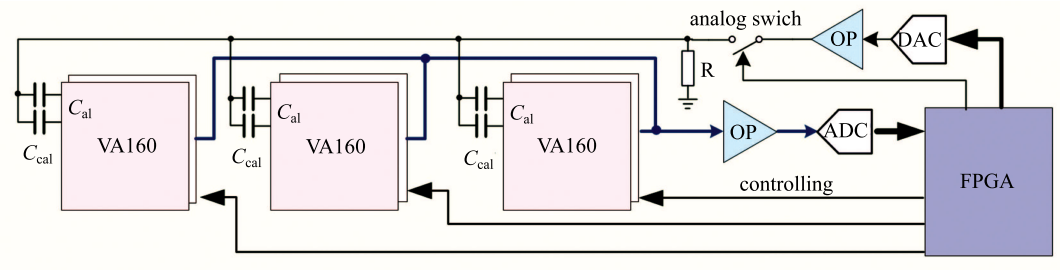

Fig. 8. (color online) Block diagram of the calibration circuit.

3.3 Calibration timing sequence

The calibration timing sequence is shown in Fig. 9. A high level of "Cali_en" sets the VA160s into calibration mode, and they then wait for triggers. After a fixed delay behind a trigger, the FPGA turns the analog switch from off to on. An exponential decay signal then appears on the "Cal" input of the VA160s.

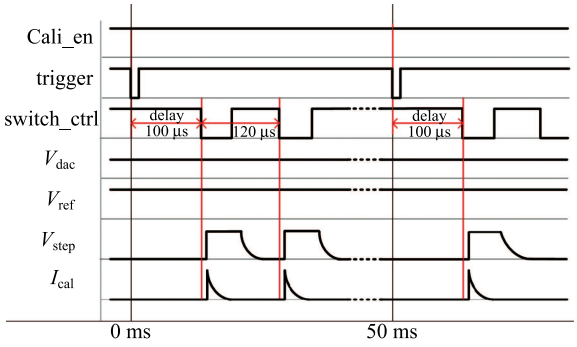

Fig. 9. (color online) Calibration timing sequence.

The calibration circuit is responsible for calibrating all channels on the FEE, but it can only calibrate one channel at a time. So two 32-bit shift registers within the VA160 are used to switch between channels and several VA160s are connected in a daisy chain.

The triggers are produced by PDPU periodically. The trigger cycle is about 50 ms. After receiving a trigger, all channels on the FEE will be calibrated in sequence. It takes 120 μs for each channel. After all channels are calibrated, the FEE will package the data and send it to the PDPU.

3.4 Onboard calibration process

The onboard calibration flow chart is shown in Fig. 10. The process consists of ten steps:

(1) Power on

(2) Initialization

After being powered on, all FEEs are set into the normal mode of acquiring scientific data by default and waiting for triggers. For onboard calibration, we can set the FEEs into calibration mode by command.

(3) Set FEE into calibration mode

When it receives a calibration command, a FEE board is set into calibration mode. It will set all VA160s into calibration mode and set the calibration voltage according to the command through a DAC and then wait for triggers.

(4) Trigger

When it receives a trigger from the PDPU, a FEE board starts the calibration process. The triggers are produced by the PDPU periodically with a period of

about 50 ms.

(5) Analog switch on

After a fixed delay of about 100 μs, the FPGA turns the analog switch from off to on to produce the calibration signal.

(6) Sample and hold

After another fixed delay (1.8–2 μs), which is the shaping time of the VA160, the FPGA controls the VA160 to sample and hold the analog voltage. After being sampled and held, the analog voltage is sent out with a differential current signal. Then the differential current signal is converted to voltage through a resistance network and amplified by an instrumentation amplifier to adapt to the ADC input dynamic range.

(7) Digitization

The analog voltage is digitized by a high-precision ADC (AD976) with 16-bit resolution and 200 kSps. After finishing digitization for one channel, the FPGA controls the calibration circuit to switch to the next channel. All channels on a FEE share a common ADC.

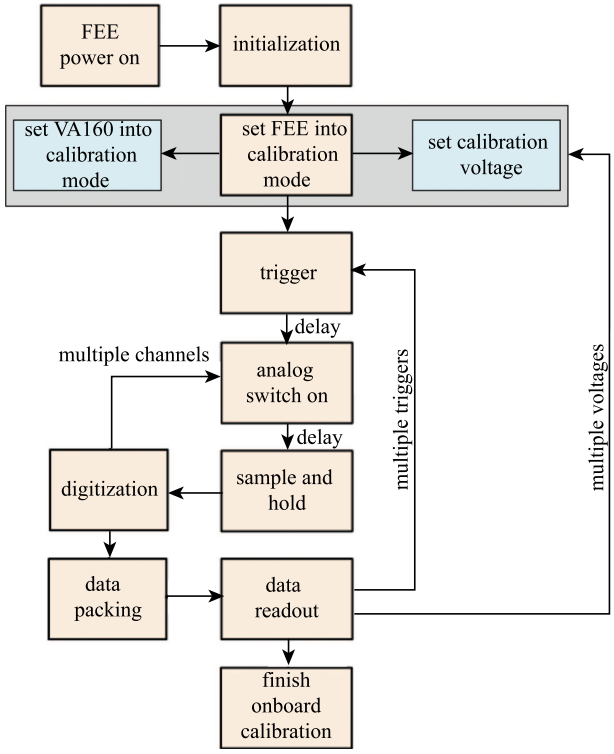

Fig. 10. (color online) Onboard calibration flow chart.

(8) Data packing

After being digitized, all data of a trigger is packed together and a 16-bit CRC (Cyclic Redundancy Check) check code added.

(9) Data readout

Finally, the data packet is sent out to the PDPU through the user-defined serial data bus. Only after the data packet of a trigger is sent out can the FEE receive the next trigger and repeat the calibration process. After finishing all triggers at one voltage, the FEE goes back to process calibration at the next voltage.

(10) Finishing onboard calibration

When calibration processes at all voltages are finished, the onboard calibration is finished.

3.5 Highly stable power supply

A highly stable power supply scheme is designed to ensure a stable property for the calibration circuit. The FEE needs three power supplies, +5.7 V, +3.4 V, −3.3 V, which are converted from the satellite's 28 V power bus with some switching power modules. Firstly, the FEE's three input power supplies are designed with high stability (drift within +/−0.1 V) according to the design specification. Secondly, the power supplies for the VA160, VATA160, ADC and DAC are converted by low dropout regulators from the three input power supplies. Thirdly, the reference voltage for ADC and DAC is supplied by an ultra-stable voltage reference chip, AD580. These designs ensure a stable property for the FEE and its calibration circuit.

4 Test results

4.1 Linearity of the calibration signal

As shown in Fig. 11, the X-axis is the calibration DAC code and the Y-axis is voltage of the calibration signal. The voltages are measured at the analog switch output ($V_{\rm ref}$) with an avometer. The calibration signal achieves a large dynamic range of over 3000 mV (equivalent to 30 pC) and a good linearity (nonlinearity is less than 0.02%). The charge dynamic range of the calibration signal covers the VA160's input range.

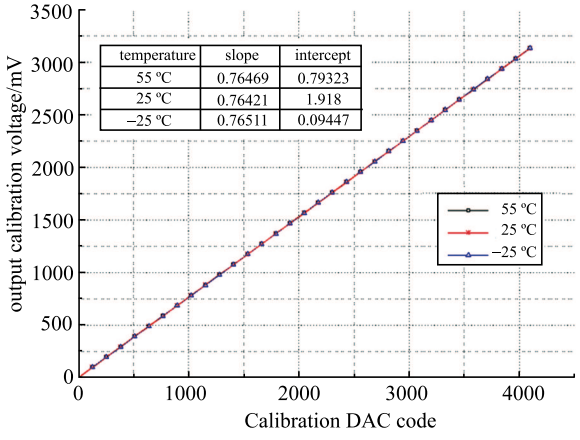

Fig. 11. (color online) Linearity of the calibration signal.

More importantly, we test the calibration circuit at different temperatures, 55 ℃, 25 ℃and −25 ℃. The test results are nearly the same and their curves are coincident. The drift of the curve slope is smaller than 0.1%

from −25 ℃to 55 ℃. This means the calibration circuit is not sensitive to temperature, so we can calibrate the front-end electronics accurately and in real-time.

4.2 Onboard calibration

The onboard calibration results of one channel are shown in Fig. 12 and Fig. 13. Figure 12 shows the linear fitting curve with data below 13 pC ($V_{\rm ref}C_{\rm cal}$). Figure 13 shows the RMS of all channels on a FEE at one calibration point which represents the noise of the calibration circuit. The test results tell us the calibration circuit achieves a high resolution of less than 5 fC.

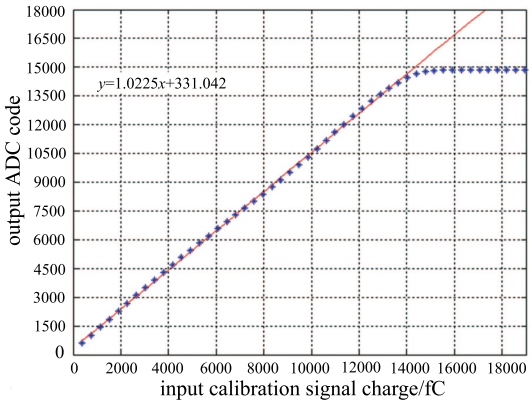

Fig. 12. (color online) Linear fitting of the calibration curve.

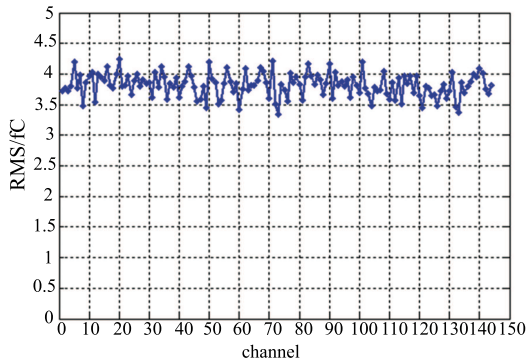

Fig. 13. (color online) RMS of onboard calibration.

4.3 Compensating with onboard calibration at different temperatures

The temperature changes rapidly along the satellite's orbit from sunrise to sunset. For the BGO calorimeter read-out electronics, its environmental temperature changes from −15 ℃ to 30 ℃ inside the satellite. Because the temperature variation may interfere with the VA160s, we need to have a good understanding of the electronics performance at different temperatures. Through real-time onboard calibration, we can learn about the FEE performance under all conditions and compensate the scientific data offline with the calibration results.

An external signal test with a function generator (Tek AFG3252) is carried out to simulate acquiring the charge of the dynode signals. Figure 14 shows the test results of one channel at different temperatures (−25 ℃, −15 ℃, 0 ℃, 25 ℃ and 55 ℃). It shows that the gain coefficient decreases with temperature.

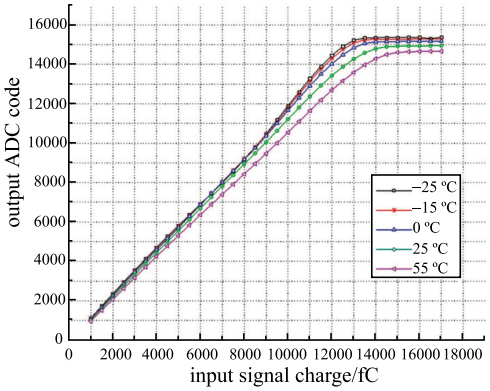

Fig. 14. (color online) External signal test at different temperatures.

We calibrate the FEE with the onboard calibration circuit at different temperatures. Calibration results of the same electronics channel at different temperatures are shown in Fig. 15. The gain coefficient has the same trend as the external signal test. Therefore it is effective to compensate the scientific data with onboard calibration results.

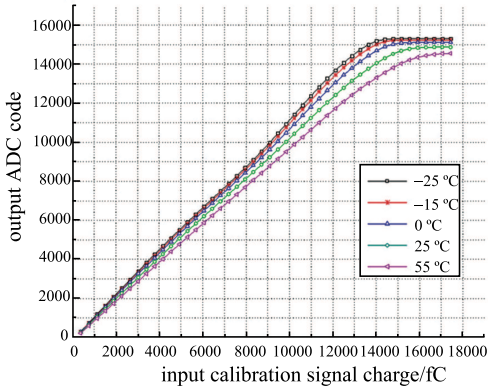

Fig. 15. (color online) Onboard calibration results at different temperatures.

The data are compensated according to the calibration result at room temperature (25 ℃). Firstly, we calculate the abscissas with the scientific data according to the calibration curves at different temperatures. Secondly, we find the ordinates with the calculated abscissas according to the calibration curves at room temperature. The calculated ordinates are the compensated data which we want.

Figure 16 shows the external signal test curves at different temperatures after compensation. The X-axis is the equivalent input signal charge and the Y-axis is the output ADC code. After compensation, all curves coincide with the one at room temperature.

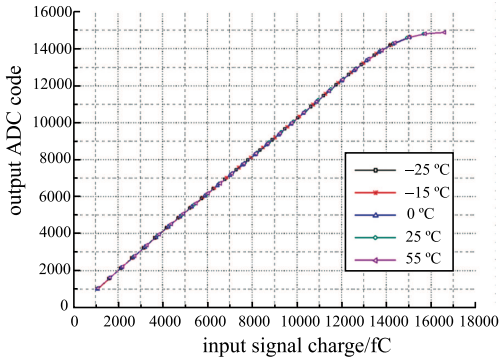

Fig. 16. (color online) External signal test results after compensated with onboard calibration.

Table 1 shows the gain coefficients and INL (integral nonlinearity) of the external signal test at different temperatures before and after compensation with onboard calibration. The results show us that, after compensation, all gain coefficients are nearly equal and a better INL is achieved. Compensating the scientific data with onboard calibration results is effective.

Table 1. Gain and INL of external signal test before and after compensation.

	before compensation		after compensation	
	gain	INL	gain	INL
−25 ℃	1.200	1.84%	1.026	0.59%
−15 ℃	1.192	1.39%	1.026	0.58%
0 ℃	1.176	0.85%	1.025	0.58%
25 ℃	1.129	0.94%	1.025	0.58%
55 ℃	1.060	0.55%	1.025	0.58%

4.4 Onboard calibration for trigger function

Another function of the calibration circuit is a self-test for the TA160's trigger function. We use the calibration of the VA160 to check the hit signal generating channels of TA160. When starting TA160 calibration, we set $Q_{\rm cal}$ (calibration signal charge) and $Q_{\rm thr}$ (TA160's hit signal threshold) as desired and set the FEE into TA160 calibration mode by remote command. After receiving triggers, the calibration circuit sends calibration signals into the VA160 and then the TA160 will generate hit signals. The FPGA receives and counts the hit signals. When $Q_{\rm cal}$ is higher than $Q_{\rm thr}$, the number of hit signals will be equal to the number of triggers. When $Q_{\rm cal}$ is lower than $Q_{\rm thr}$, the number of hit signals will be zero. If not, there is a problem with the corresponding hit signal generating channel. During TA160 calibration, the FEE does not generate calibration data.

5 Conclusion

An onboard calibration circuit has been designed on the BGO FEE. It can calibrate the front-end electronics channels and help us check the status of every charge measurement channel and hit signal generating channel. We also can compensate the scientific data offline with the onboard calibration results. Test results showed that the onboard calibration circuit has a good performance: wide dynamic range (0–30 pC), good resolution (5 fC) and good linearity, which meets the requirements for the FEE. The temperature drift can be compensated through onboard calibration. Now the calibration circuit is successfully operating on the BGO calorimeter read-out electronics in the DAMPE Qualification Model and Flight Model. The DAMPE satellite was launched at the end of 2015 and the calibration circuit will play an important role in orbit.

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