Improvement of the Radiation Hardness of SIMOX Buried Oxides by Silicon Ion Implantation

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Abstract The total dose response characteristics of the buried oxides (BOX) in separation by implanted oxygen (SIMOX) silicon-on-insulator (SOI) wafers have been improved by implanting silicon ion into the BOX layers. NMOS/SOI transistors with enclosed-gate structure fabricated in SIMOX wafers were exposed to ^{60}Co γ-ray radiation. The total-dose radiation hardness of the BOX layers is characterized by the current voltage (I-V) measurements. The experimental results show that the implantation of silicon ion into the BOX layers can greatly reduce back channel threshold voltage shifts ($\Delta V_{\rm th}$), which increase the BOX layer hardness to total-dose irradiation.

Key words silicon on insulator, ion implantation, total-dose radiation effect, threshold voltage shift

1 Introduction

Due to buried dielectric isolation, SOI CMOS devices have smaller leakage current and higher speed performance and larger device density than conventional bulk silicon CMOS devices. However, the buried layers make hardening SOI devices to total-dose irradiation difficult. The presence of the radiation induced trapped holes in the buried layers can cause a parasitic back-channel conduction path for NMOS/SOI. Therefore, it is necessary to harden the buried layers so that the SOI devices can operate reliably in a higher radiation environment.

The new research results of the hardened SOI buried layers formed by silicon ion implantation have been reported to reduce the positive charge trapped in the oxide during exposure to ionizing radiation[1]. In this paper, we further discuss the basic mechanism responsible for the reduction of $\Delta V_{\rm th}$. The improved total-dose radiation hardness of the BOX layers has been observed by silicon ion implantation and high temperature anneal.

2 Experiment details

2.1 Devices

The NMOS transistors were fabricated on SIMOX wafers for this study with a buried oxide thickness of 375nm and top silicon thickness of 200nm, which is appropriate for scaled deep sub micron devices. One wafer was improved by implanting silicon at a dose of 1×10^{15}cm^{-2} and then annealed at 800℃ in N_2 ambience, the other wafer was not implanted. The processing steps include isolation, well definition, gate oxidation, poly-silicon gate definition, lightly doped drain (LDD), source/drain implant, contact cut, and first metal. Gate length is 3μm and uses a LOCOS oxide for transistor isolation. Enclosed-gates (Fig. 1) are employed in the tested devices on both improved and unimproved samples. For the enclosed-gate transistors, radiation-induced field-oxide parasitic leakage current does not contribute to back-gate transistor leakage current, so the field-oxide parasitic leakage does not affect investigations of the buried oxide[2].

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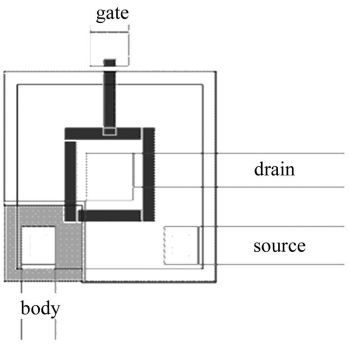

Fig. 1. Layout and circuit of NMOS/SOI transistor.

2.2 Radiation sources

The ^{60}Co γ-ray irradiations were performed at the Northwest Institute of Nuclear Technology (NINT). Transistors were irradiated at a dose rate of 240—250rad(Si)/s for ^{60}Co irradiations. *I-V* characteristics of back channel transistors were measured using a computer controlled HP4156A parametric analyzer before and after irradiation. Each measurement was taken within 20 min after irradiation at each dose. The back-gate *I-V* curves were analyzed for $\Delta V_{\rm nit}$ and $\Delta V_{\rm not}$ using the sub threshold current-voltage separation technique[3].

3 Results and discussion

For the radiation test, threshold voltage shifts as a function of total dose are used to characterize the devices irradiated with the worst-case bias. The largest shift of back channel threshold voltage occurs under the pass-gate bias condition[4] as following: $V_{\rm gate}=V_{\rm body}=V_{\rm substrate}$=0V, $V_{\rm source}=V_{\rm drian}$=5V. Then we set $V_{\rm source}=V_{\rm gate}=V_{\rm body}$=0V, $V_{\rm drian}$=0.1V, and scanned $V_{\rm substrate}$ from −30—40V to measure the $I_{\rm ds}$-$V_{\rm gs}$ of the back channel transistor. The experimental results of the back channel radiation response of *I-V* characteristics under pass-gate irradiation biases at dose of 0, 100, 500krad(Si) and 1Mrad(Si) are shown in Fig. 2 and Fig. 3.

Comparing Fig. 2 with Fig. 3, the improved sample has less back-gate threshold voltage shift than the unimproved one at any irradiation dose. It demonstrates that silicon ion implantation can effectively harden the transistors below 1.5Mrad(Si) irradiation, and prevent them from failure induced by threshold voltage shift of the back gate transistor. The back channel threshold voltage shift is due to the Si/SiO_2 interface traps ($\Delta V_{\rm nit}$) and the positive charged trapped oxide holes ($\Delta V_{\rm not}$). To further study the mechanism responsible for this reduce of shift in the $\Delta V_{\rm th}$, we extracted $\Delta V_{\rm th}$ from $I_{\rm d}$-$V_{\rm d}$, characteristics at a drain current $I_{\rm d}$=10^{-6}A., then divided it into $\Delta V_{\rm nit}$ and $\Delta V_{\rm not}$, shows in Fig. 4, as a function of radiation dose, where $\Delta V_{\rm th}=\Delta V_{\rm nit}+\Delta V_{\rm not}$[3].

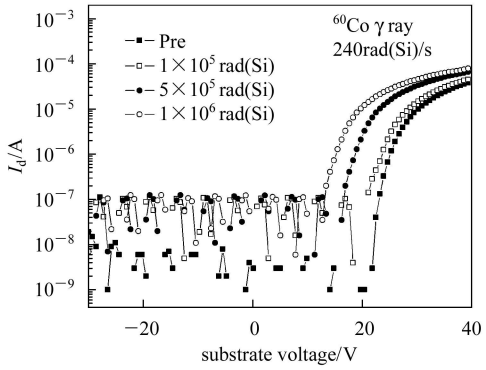

Fig. 2. Back channel $I_{\rm ds}$-$V_{\rm gs}$ curves of improved NMOS/SOI after different total dose irradiation.

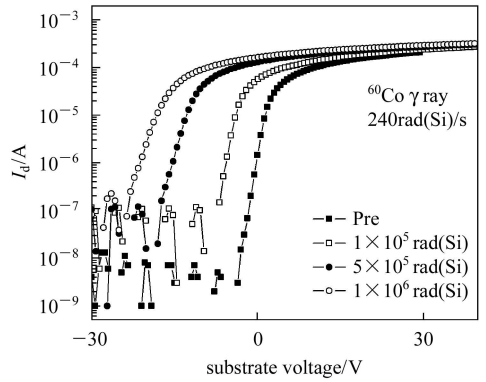

Fig. 3. Back channel $I_{\rm ds}$-$V_{\rm gs}$ curves of unimproved NMOS/SOI after different total dose irradiation.

Figure 4 shows the evidence that silicon ion implantation could reduce the voltage shift due to positive charged trapped-oxide holes. The curves indicate that the existence of the radiation-induced trapped holes in the BOX, rather than that of the radiation-induced interface-trapped charges, is a key factor affecting the threshold voltage of back channel. The effect of the radiation-induced interface-trapped charges on the radiation hardness of the BOX layers is negligible as compared to that of the radiation-induced trapped holes.

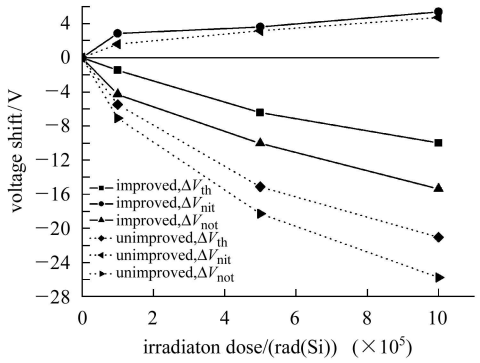

Fig. 4. Threshold voltage and contributions to that shift due to interface traps and trapped-oxide charge calculated from the sub threshold-current curves in Fig. 2 and Fig. 3.

Once $\Delta V_{\rm not}$ is known, the increase in the number of trapped charges in the oxide can be calculated by

$$\Delta N_{\rm ot} = \frac{\Delta V_{\rm not} \times \varepsilon_{\rm ox}}{t_{\rm ox} \times q},$$

The values of $\Delta N_{\rm ot}$ calculated in Origin 7.0 during the fitting of Fig. 4 are given in Table 1. It is clearly demonstrated that the improved transistors have smaller saturated trapped charges density $\Delta N_{\rm ot}$.

The mechanism is that in silicon ion implanted oxides, there are entities that have a large electron capture cross section. Photoluminescence studies[5] indicate that these entities are silicon nanoclusters. When these implanted oxides are exposed to ionizing radiation, nanoclusters cause the formation of electron traps in the oxide, and electrons trapped at these sites can compensate the positive charge of the trapped holes.

Table 1. The calculated values of $\Delta N_{\rm ot}$.

	improved	unimproved
0 rad(Si)	0	0
100krad(Si)	2.47883×10^{11}	4.06723×10^{11}
500krad(Si)	5.7711×10^{11}	1.05013×10^{12}
1M rad(Si)	8.83531×10^{11}	1.47931×10^{12}

4 Conclusions

In this paper, we have made an improvement of the radiation hardness of SIMOX buried layers by the implantation of the silicon ion into the SIMOX buried layers. According to the above experimental results and detailed discussion, when compared to commonly unimproved NMOS/SOI transistors, the improved transistors have smaller saturated trapped charge density resulting from total dose radiation, and the voltage shift due to positive charged trapped-oxide holes is greatly reduced.

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采用硅离子注入改进SIMOX埋氧的抗总剂量辐射性能研究

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摘要 采用硅离子注入工艺对注氧隔离(SIMOX)的绝缘体上硅(SOI)材料进行改性, 在改性材料和标准SIMOX材料上制作了部分耗尽环型栅NMOS/SOI晶体管, 并对其进行^{60}Co γ射线总剂量辐照试验. 通过背栅的*I-V*特性表征晶体管的总剂量辐照特性. 结果表明, 在埋氧层注硅可以降低NMOS/SOI受辐照引起的背栅阈值电压漂移, 提高埋氧层的抗总剂量能力.

关键词 绝缘体上硅 离子注入 总剂量辐射效应 阈值电压漂移

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