Clock distribution for BaF_2 readout electronics at CSNS-WNS *

Bing He(何兵)[1,2] Ping Cao(曹平)[1,2;1)] De-Liang Zhang(张德良)[1,3]
Qi Wang(王奇)[1,3] Ya-Xi Zhang(张雅希)[1,3] Xin-Cheng Qi(齐心成)[1,2] Qi An(安琪)[1,2]

[1] State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, Hefei 230026, China
[2] School of Nuclear Science and Technology, University of Science and Technology of China, Hefei 230026, China
[3] Department of Modern Physics, University of Science and Technology of China, Hefei 230026, China

Abstract: A BaF_2 (Barium Fluoride) detector array is designed to precisely measure the (n, γ) cross section at the CSNS-WNS (white neutron source at China Spallation Neutron Source). It is a 4π solid angle-shaped detector array consisting of 92 BaF_2 crystal elements. To discriminate signals from the BaF_2 detector, a pulse shape discrimination method is used, supported by a waveform digitization technique. There are 92 channels for digitizing. The precision and synchronization of clock distribution restricts the performance of waveform digitizing. In this paper, a clock prototype for the BaF_2 readout electronics at CSNS-WNS is introduced. It is based on the PXIe platform and has a twin-stage tree topology. In the first stage, clock is synchronously distributed from the tree root to each PXIe crate through a coaxial cable over a long distance, while in the second stage, the clock is further distributed to each electronic module through a PXIe dedicated differential star bus. With the help of this topology, each tree node can fan out up to 20 clocks with 3U size. Test results show the clock jitter is less than 20 ps, which meets the requirements of the BaF_2 readout electronics. Besides, this clock system has the advantages of high density, simplicity, scalability and cost saving, so it can be useful for other clock distribution applications.

Keywords: CSNS-WNS, BaF_2 detector array, clock system, PXIe readout electronics

PACS: 29.85.Ca **DOI:** 10.1088/1674-1137/41/1/016104

1 Introduction

The China Spallation Neutron Source White Neutron Source (CSNS-WNS) is a scientific facility in Dongguan, China. It can provide intense flux, good energy spectrum and great resolution neutrons [1]. The BaF_2detector array (Fig.1) is a 4π detector array consisting of 92 crystal elements in the WNS. Its main purpose is to measure the cross section of the (n,γ) reaction. To discriminate the signals form the BaF_2 detector, pulse shape discrimination is used, supported by a waveform digitization technique based on high performance ADCs [2]. To deal with the massive quantity of data produced, the readout electronics is distributed in 4 PXIe crates, and a clock system is also required to provide low jitter and low skew clocks. The PXIe platform can bring great advantages for the design of readout electronics. However, it brings a challenge for the clock distribution. Traditionally, clocks are fanned out to modules through fiber or differential cable from the front panel of the readout module. However, these schemes would be difficult because of the limited 3U size of the PXIe module. In this paper, a distributed clock system based on PXIe crates is proposed. It can transmit high-quality clock through coaxial cable with 2 m length between crates. Besides, precise clock can also be distributed to each slot in the crate without any extra cables. Furthermore, this clock system has advantages of scalability, availability, space and cost-saving [3, 4].

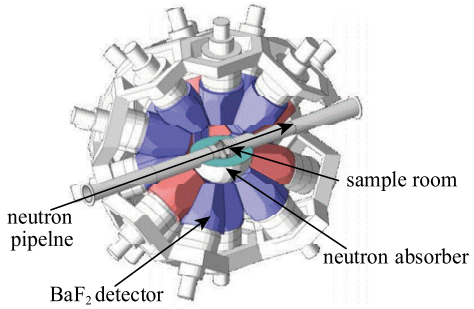


Fig. 1. (color online) BaF_2 detector array.

Generally, the clock is distributed from a global node and fanned out to each receiving slave node. For the end-

Received 24 February 2016
∗ Supported by National Research and Development plan (2016 YFA0401602) NSAF (U1530111) and National Natural Science Foundation of China (11005107)
1) E-mail: cping@ustc.edu.cn

cap time of flight (TOF) upgrade of the Beijing Spectrometer (BESIII), two types of VME 9U module are used to distribute clock. One is assigned as the master clock module and the others are slave clock modules. Master and slave modules are located in two VME crates respectively. The master clock module transmits clock to slave clock modules by fiber because of the long distance between crates. Furthermore, once received by a slave module, clock is distributed to all readout electronic modules in the same crate through differential cables from the front panel of the slave module [5–7].

In the case of the nTOF experiment at CERN, the sampling clocks are generated by a central clock generator and are distributed to digitizer modules via fan-out units (integral parts of the generator) by equal length cables. These digitizer modules are located in 19 CPCI crates. Care has been taken to assure that the skew of each output is less than 200 ps in respect to all other outputs [8].

For the clock system of GTAF (gamma-ray total absorption facility) at the Chinese Institute of Atomic Energy, all commercial digitizers (acqiris DC271A) are located in one CPCI crate. The reference clock is transmitted to one digitizer at first, then this digitizer distributes clocks further to other digitizers via ASBus (Auto-Synchronous Bus) that can distribute clock signals along a plug-in front panel bus. Up to 7 digitizers can be synchronized with the ASBus [9].

For the case of the BaF_2 detector array at CSNS-WNS, the readout electronics is designed based on PXIe platform because of its high data transmission capacity. The up to 8 GB/s of signal-slot transfer bandwidth can guarantee the ability to upload the massive data volume produced by waveform digitizing to the crate controller in real-time and in parallel. However, the size of the PXIe module causes problems for clock distribution. The 3U euro PXIe module is about 90 mm, but it should fan out at least 18 channels for the case of BaF_2 readout electronics. Moreover, even more serious is that trigger distribution also needs module panel space. So there is no space for photoelectric converters or differential cable connectors if a traditional clock distribution method is used. To solve these problems, a high-density clock distribution method based on the PXIe platform is proposed in this paper.

2 Architecture of the clock system

The clock distribution network has a tree-like topology, as illustrated in Fig. 2. A global clock module is appointed as the root of this tree, while each PXIe module is appointed as a clock-receiving node in this tree.

The clock distribution tree has a twin-stage structure. In the first stage, the global clock module distributes clock to local clock modules in each PXIe crate. The clock loopback is used to correct the phase error that is caused by different transmission paths. In the second stage, clock modules will fan out clocks to other modules in the same crate, acting as a buffer.

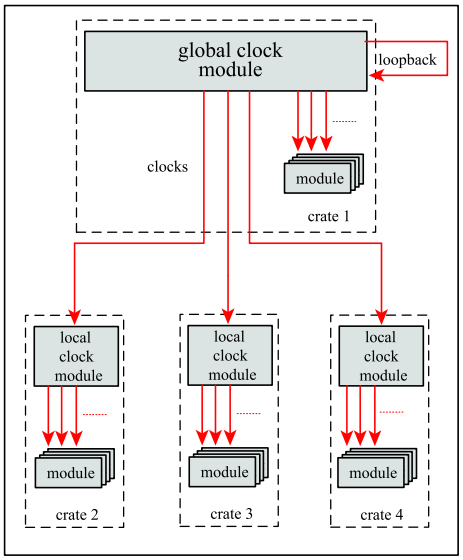


Fig. 2. (color online) Clock distribution tree.

In addition, in consideration of compatibility with PXIe backplane clocking resources [10], the frequency of the clock system is 100 MHz. Actually, the 12 bit ADC for waveform digitization runs at a sampling rate of 1000 MSps, which needs a reference clock with low jitter and low skew. In order to ensure the accuracy of clock distribution, the clock jitter and clock skew should be less than 100 ps. However, in practice a few design challenges are involved in this approach:

(1) Transmitting clocks from the global clock module to local clock modules over 2 m distance with limited panel space. The clock skew and jitter should be calibrated at the same time.

(2) Distributing clocks to all 16 slots in a crate through a 3U size clock module with high quality.

3 Clock system implementation

3.1 Clock distributing between crates

The global and local clock modules are the main components of the clock distribution. They are both 3U size and compatible with the PXIe specification. After being installed in the BaF_2 readout electronics, the global clock module distributes clock (from the CSNS accelerator or on-board itself) to all local clock modules synchronously. While receiving the transmitted clock from global module, the local module distributes clock synchronously further to each readout electronics module through the high performance backplane inside the same

crate. To guarantee the ability of fanning the clock out between and inside crates, the total fanning number can reach up to 20 for the global clock module.

For the clock distribution between crates, fibers and differential cables are not appropriate because of the shortage of panel space. So coaxial cable should be used to transmit clocks to local clock modules, and micro-miniature coaxial (MMCX) connectors are used to save panel space further. But coaxial cable inevitably introduces another problem, signal distortion, especially for long transmission distance and high frequency. So a new technique should be used to overcome this difficulty.

Generally, a signal transmission channel can be considered as a low-pass filter, which can attenuate high frequency signals more seriously than low frequency signals. Longer distance and higher frequency means more serious attenuation. For transmitting a high precision global clock, this low-pass filter obviously degrades the signal quality, which can further degrade the precision and synchronization of the global clock distribution for the experiment. So the signal quality should be improved before it is used in the local clock module. Equalization is a technique to compensate the attenuated high frequency components in signals [11]. In Fig. 3, after transmission over a long cable, the signal is seriously distorted at the receiver side. An equalizer can be used to filter the noise, compensate the attenuated components and generate good quality signal out.

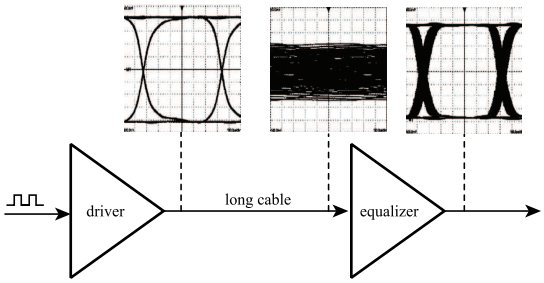


Fig. 3. An equalizer improves the signal quality.

So equalizers can be used in this clock system to improve the clock quality received by local clock modules. The driver and equalizer should be considered as a pair for signal transmission. They can extend the valid transmission distance over long single-ended media. The driver is a high-speed differential buffer with adjustable output amplitude, while the equalizer is optimized for equalizing signal transmitted over balanced copper cable. However, the lowest working frequency of the equalizer is 150 MHz, so the clock transmitted between the crates should be upgraded to 200 MHz instead. The clock link via coaxial cable is shown in Fig. 4 [12].

As discussed above, clock skew is also a critical factor for clock distributing. Clock skew introduced by the length difference of cables should be eliminated or calibrated. The simplest way to eliminate skew is to make the lengths of all the distribution cable the same, but this is troublesome and time consuming. A phase-locked loop (PLL) with adjustable delay can be used to correct the clock skew. The PLL clock output delay can be configured individually by a FPGA with a minimum step of 25 ps. So it is convenient to compensate the clock skew by reconfiguring the PLL with high efficiency and accuracy.

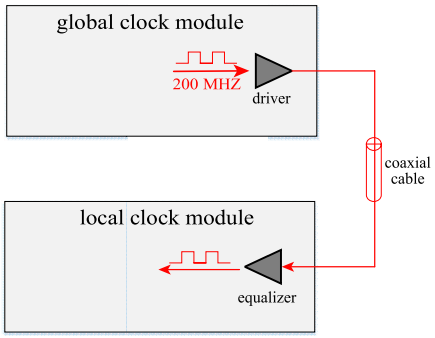


Fig. 4. (color online) Clock distribution via coaxial cable.

3.2 Clock distribution inside a crate

To distribute the clocks to 16 slots in a 3U PXIe crate, fanning out by extra cables is not suitable because of the shortage of panel space. A scheme to distribute high-quality clocks without the use of cables should be adopted.

PXIe crate provides three kinds of slot: a system controller slot, a system timing slot (STM) and 16 peripheral slots. It also provides rich backplane traces with high performance for trigger and synchronization. The PXIe_DSTARA is a differential star trigger bus designed to distribute point-to-point, high-quality LVPECL clocks from the STM slot to each peripheral slot. The maximum clock skew of the two signals within PXIe_DSTARA is less than 25 ps, while the jitter introduced to the clock is less than 5 ps.

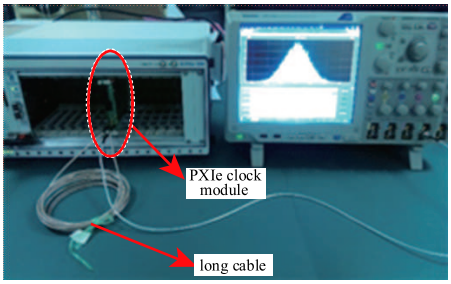
So PXIe_DSTARA can be used to distribute clocks to each slot inside the crate. The time module is located in the STM slot, while digitizing modules are located in peripheral slots. Based on this scheme, up to 16 clocks can be distributed synchronously over the differential star trigger bus. Furthermore, this scheme is convenient, concise, space saving and meets the quality requirements of the readout electronics.

4 Experiment and verification

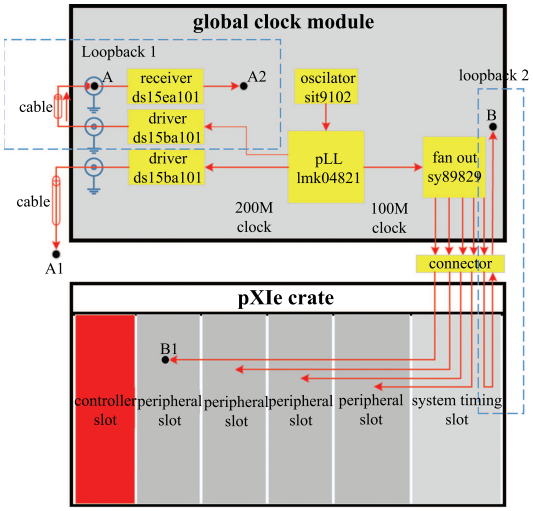
4.1 Test platform

According to this proposed clock distribution structure, to evaluate the clock quality, a test platform has been constructed with a global clock module and a PXIe

crate as shown in Fig. 5. The global clock module (shown in Fig. 6) is located in the STM slot of the crate through the backplane connector. In the global clock module, the PLL would produce high-quality 100 M and 200 M LVDS clocks sourcing from the oscillator. Then the 200 MHz clocks are fanned out through cables, while the 100 MHz clocks are distributed through PXIe_DSTARA on the backplane.



(1) photograph of platform



(2) diagram of platform

Fig. 5. (color online) Test platform.

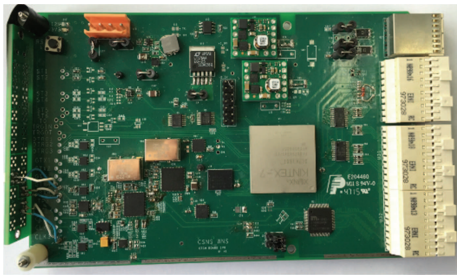


Fig. 6. (color online) global clock module.

As illustrated in Fig. 4, two loopbacks are used to simulate the clock distribution between and within crates. There are five test points (A, A1, A2, B, B1) used to measure the quality of this clock distribution system.

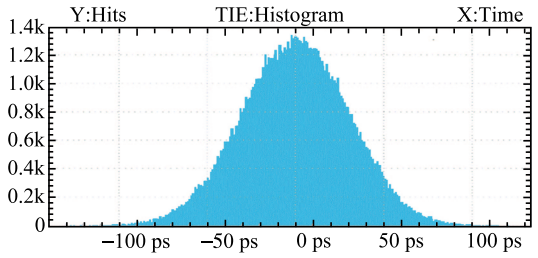
Loopback 1 simulates the clock distribution process between crates. The clock can be transmitted back to the global clock module through this loopback channel. In Fig. 4, signal A denotes the single-ended clock received by the local clock module. Signal A2 represents the differential clock after being equalized. To evaluate clock skew between crates, signal A should be compared with signal A1, denoting clock distributed to other crates.

In loopback 2, the clocks would be fanned out with the LVPECL signalling technique to each slot through the dedicated PXIe_DSTARA backplane bus. One PXIe_DSTARA would trace back to the global clock module through the backplane. Signal B is the clock received by each slot. For the clock skew measurement, the skew between clock B and clock B1 should be measured.

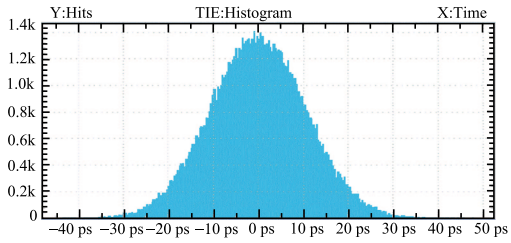
4.2 Test result

All data about the quality of the clock distributing system is measured and acquired by a Tektronix DPO5104 oscilloscope. The jitter of the distributed clock is characterized in TIE (Time Interval Error) at a population of 10^5, which is enough to get a highly accurate statistical result.

Test results of clock performance are shown in Fig. 7, from which three conclusions can be drawn. The first conclusion is that the clock jitter of A2 and B is less than 20 ps, which meets the requirement of the readout electronics. The second is that the clock jitter has been corrected from 30 ps to 10 ps by the equalizer, which demonstrates that distributing clock over coaxial cable combined with an equalizer can achieve high-quality clock distribution over 2 m distance. The third conclusion is that the precision of clock phase difference between A2 and B is 19 ps, which shows that the clock



(a) Jitter of A, TIE=30 ps



(b) Jitter of A2, TIE=10 ps

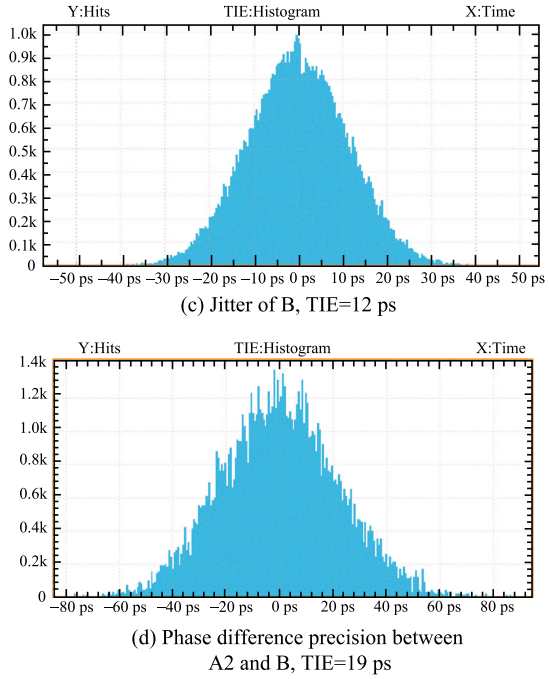


Fig. 7. (color online) Clock performance.

can be distributed with excellent synchronization performance.

5 Conclusion

An optimized clock distributing system with high performance and density has been designed for the CSNS-WNS BaF_2 readout electronics. Long coaxial cable, equalizer and PXIe dedicated differential bus are used to distribute clocks synchronously and precisely. Test result shows that the clock jitter is less than 20 ps, which meets the requirements of the readout electronics. It is a breakthrough that only 4 PXIe modules are used to distribute clocks to 68 modules. Compared with traditional clock distribution techniques, this clock system has the advantages of scalability, availability, space and cost saving. This synchronous clock distribution method can also be used in other applications which require precise clock distribution.

The authors gratefully acknowledge all members of CSNS-WNS for their earnest support and help during the work.

References

1 J. Y. Tang, S. N. Fu, H. T. Jing et al, Chin. Phys. C, **34**(1): 121–125 (2010)
2 C.M. Combes, P. Dorenbos, R.W. Hollander, C.W.E. van Eijk, Nucl. Instr. Meth. A, **416**: 364–370 (1998)
3 S. X. Fang, S. N. Fu, Q. Qin et al, J. Korean Phys. Soc., **48**(4): 697–702 (2006)
4 Matsuzaki T, Ishida K, Nagamine K et al, Nucl. Instrum. Methods A, **465:** 365–383 (2001)
5 P. Cao, W. J. Sun, X. L. Ji et al, Chin. Phys. C, **38**(4): 046101-1∼9 (2014)
6 H. Li, S. B. Liu, C. Q. Feng et al, IEEE Trans. Nucl. Sci., **57**(2) 442–445 (2010)
7 S. Y. Wang, P. Cao, S. B Liu and Q. An, Chin. Phys. C, **39**(12): 126102-1∼5 (2015)
8 nTOF Technical Report, CERN/INTC/ 2000-018
9 Q. P. Zhong, Z. Y. Zhou, H. Q. Tang et al, Chin. Phys. C, **32**(S2): 102–105 (2008)
10 NI. Specifications, Crate NI-1085
11 Jared L. Zerbe, Carl W. Werner, Vladimir Stojanovic et al, IEEE J. Solid-st. Circ., **38**(12): 2121–2130 (2003)
12 TI. Specification, Model DS15EA101