An ultrafast front-end ASIC for APD array detectors in X-ray time-resolved experiments *

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Abstract: An ultrafast front-end ASIC chip has been developed for APD array detectors in X-ray time-resolved experiments. The chip has five channels: four complete channels and one test channel with an analog output. Each complete channel consists of a preamplifier, a voltage discriminator and an open-drain output driver. A prototype chip has been designed and fabricated using 0.13 μm CMOS technology with a chip size of 1.3 mm × 1.9 mm. The electrical characterizations of the circuit demonstrate a very good intrinsic time resolution (rms) on the output pulse leading edge, with the test result better than 30 ps for high input signal charges (> 75 fC) and better than 100 ps for low input signal charges (30–75 fC), while keeping a low power consumption of 5 mW per complete channel.

Keywords: time-resolved, APD, ASIC, synchrotron X-ray

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1 Introduction

Silicon avalanche-photodiode (APD) detectors have a number of advantages, such as high count rate, large dynamic range, and nanosecond or faster time resolution. They have been used in time-resolved experiments with pulsed synchrotron X-rays, such as nuclear resonance scattering (NRS) experiments [1, 2] and laser pump/X-ray probe experiments [3], for more than two decades. However, traditional time-resolved APD detectors [4–8] only have a single APD sensor and adopt a commercial circuit or discrete element circuit to read out the weak signal output by the APD sensor. In order to acquire a larger reception solid angle, higher count rate and higher integration density, it is necessary to develop an APD array detector for X-ray time-resolved experiments.

We are now developing an APD array detector for the High Energy Photon Source Test Facility (HEPS-TF) project. This is an R&D project for the planned future High Energy Photon Source (HEPS) in Beijing, China. The goal of the detector design is as follows. To get an active area of 1 cm^2, the array size is 10 × 10, with a pixel size of 1 mm × 1 mm. The pixel has a reach-through structure and the absorption layer thickness is about 100 μm. So the time resolution of the detector, the full width at half maximum (FWHM), can be of the order of 1 ns, corresponding to a root mean square (rms) resolution of 0.426 ns. Ten CMOS ASICs (ten channels each) will be used to read out the pixel array signals.

This paper presents a prototype ASIC chip for the APD array detector. The prototype chip includes five channels: four complete channels and one test channel with an analog output. Each complete channel consists of a preamplifier, a voltage discriminator and an open-drain output driver. The readout noise and the power consumption are reduced by using a flipped voltage follower (FVF) as the input stage of the preamplifier. An AC coupling circuit is also employed in the preamplifier to decrease the DC offset of the preamplifier. The discriminator is based on a cascade of four low-gain and high bandwidth differential amplifiers with a hysteresis function. To match the LVDS output levels, an open-drain differential circuit is adopted as the output driver, which can configure the output level by programming external resistors. The detailed design of the prototype ASIC chip will be discussed in the following sections. Measurement results are also presented to demonstrate the capabilities of the chip. In the next step, a practical

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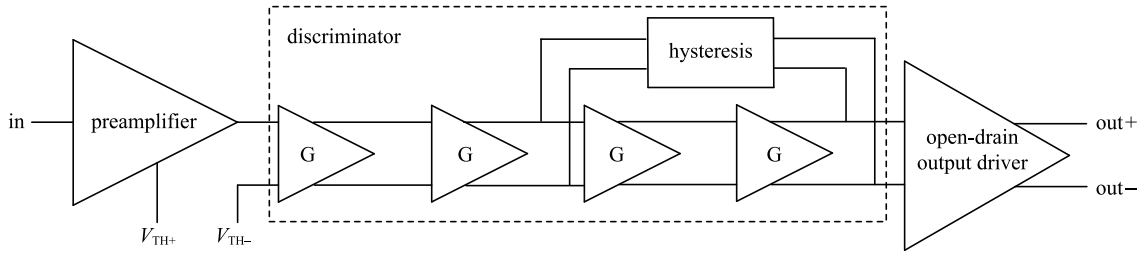

Fig. 1. Functional block diagram for one full channel of the ASIC chip.

ASIC chip with ten channels will be designed based on this prototype chip.

2 Design of the readout ASIC

In the five-channel prototype ASIC, four channels have complete functional modules for time measurement and one channel is designed for testing, with the output signal of preamplifier directly exported by an analog driver. Figure 1 shows the block diagram of one full channel. The signal path includes the preamplifier, discriminator and open-drain output driver. The preamplifier receives the current signal, output by the APD sensor, and converts it into a voltage signal. Then, the voltage signal is discriminated by the discriminator. If the voltage signal is larger than the threshold voltage, the discriminator will output a digital pulse. Finally, the digital pulse is output by the open-drain output driver with LVDS levels. Moreover, the whole chip uses a common threshold voltage, which is supplied by an off-chip module.

2.1 Preamplifier

The input stage of a traditional preamplifier [9–11] is shown in Fig. 2. The input resistance of the traditional preamplifier can be calculated as

$$R_{\text{in\_tra}} \approx \frac{1}{g_{\text{m\_in}}}, \tag{1}$$

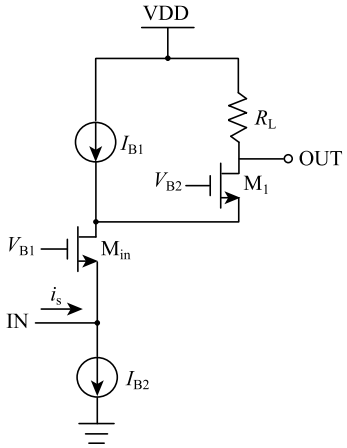

Fig. 2. Simplified schematic of the input stage of a traditional preamplifier.

where $g_{\text{m\_in}}$ is the transconductance of M_{in}.

Figure 3 shows the proposed preamplifier structure. The input stage of the preamplifier, constituted by the transistors M_1, M_2 and the current source I_{B1}, is used to receive the APD current signal i_s. The transistors M_1 and M_2 form a flipped voltage follower (FVF) [12], whose bias current is generated by I_{B1}. The feedback in the FVF results in a very low input resistance at the input terminal. The input resistance of the preamplifier can be calculated approximately using the following equation [12], and is of the order of a few tens of ohms:

$$R_{\text{in\_amp}} \approx \frac{1}{g_{\text{m1}} g_{\text{m2}} r_{\text{o1}}}, \tag{2}$$

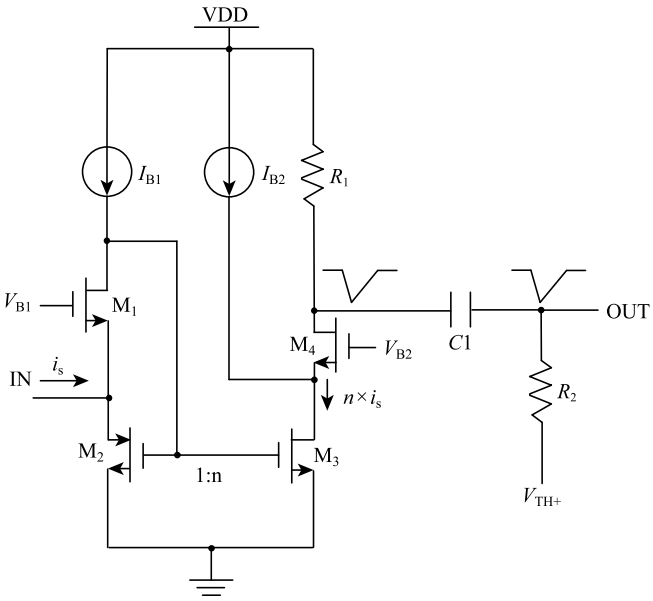

Fig. 3. Structure of the proposed preamplifier.

where g_{m1} is the transconductance of M_1, r_{o1} is the output resistance of M_1, and g_{m2} is the transconductance of M_2. If $R_{\text{in\_tra}} = R_{\text{in\_amp}}$, from Eq. (1) and Eq. (2), we can derive that $g_{\text{m1}} = \dfrac{g_{\text{m\_in}}}{g_{\text{m2}} r_{\text{o2}}}$. The dominating noise source in the traditional preamplifier is the thermal noise from the common-gate transistor M_{in}, and the dominating noise

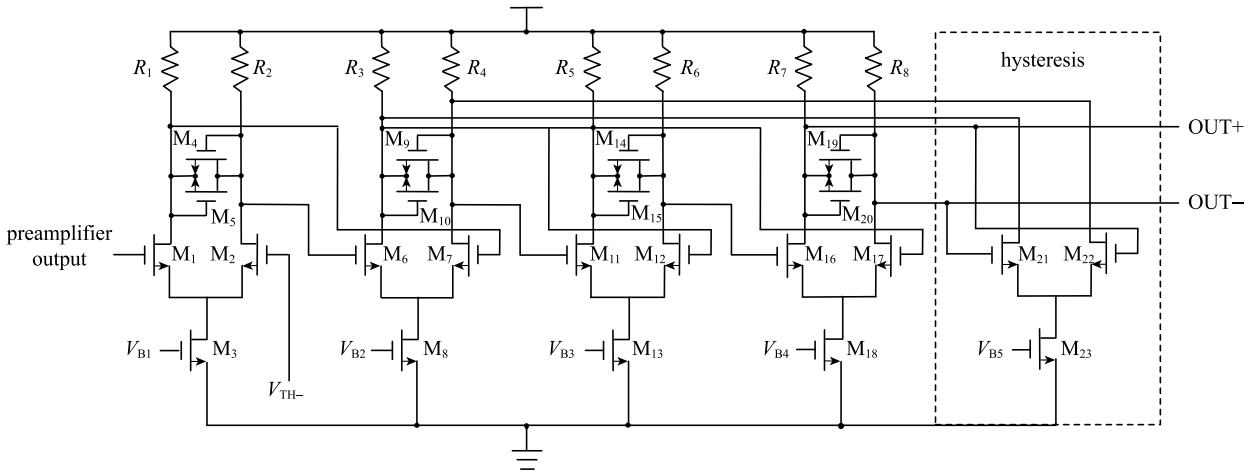

Fig. 4. Structure of the discriminator.

source in the proposed preamplifier is the thermal noise from the common-gate transistor M_1. The thermal current noise of a MOS transistor decreases with as its own transconductance (g_m) decreases [13]. Therefore, the proposed preamplifier has a lower noise performance and can detect a smaller signal than the traditional preamplifier. The transistors M_2 and M_3 compose a current mirror with a gain of n (in this design $n=6$). After being amplified by the current mirror, the signal-to-noise ratio (SNR) will be sufficiently large to make the preamplifier noise non-critical. The amplified current signal $n \times i_s$ flows through the branch made of transistor M_4 and load resistance R_1, and is converted into the voltage signal. The bias current of M_3 is provided by the current source I_{B2}, as a result of which $I_{B2} \approx n \times I_{B1}$. The capacitance C_1 and resistance R_2 constitute an AC coupling circuit. In the stationary state the baseline of the preamplifier is kept at the positive threshold V_{TH+}, so the DC offsets between the preamplifiers are eliminated. Using the AC coupling technique to fix the baseline is simpler and easier to implement than the feedback baseline restore technique in Refs. [9–11]. The AC coupling baseline holder makes it possible to set a precise threshold for the subsequent discriminator, which is a key point to discriminate the X-ray photon accurately.

2.2 Discriminator

Figure 4 shows the structure of the discriminator. The discriminator is based on a cascade of four low gain and high bandwidth differential amplifiers with resistance loads and diode-connected transistors. The diode-connected transistors are adopted to clamp the output voltages of the differential amplifiers so that the discriminator recovery time from large signals can be reduced. Besides, the amplifier (composed of transistors M_{21}, M_{22} and M_{23}) is used in a positive-feedback loop connection and introduces a hysteresis feature for the transition time to prevent oscillations. The discriminator is optimized for high speed, so relatively small transistors are used. One input of the discriminator is driven from the output of the preamplifier, while the other is connected to the negative threshold V_{TH-}. The discrimination threshold V_{TH} is defined as $V_{TH} = V_{TH+} - V_{TH-}$. V_{TH+} and V_{TH-} are set through the external references, in such a way that all channels have the same threshold value.

2.3 Output driver

Figure 5 shows the structure of the output driver. The output stage is an open-drain differential circuit which can provide large current switching between the two outputs and output fast leading edge signals. The resistances R_1, R_2 and R_3 constitute the external resistance net. We can programme the external resistance net to match the output signal to the user needs. Meanwhile, the output driver is still biased by this resistance net. In the default configuration the differential output signals comply with the LVDS protocol.

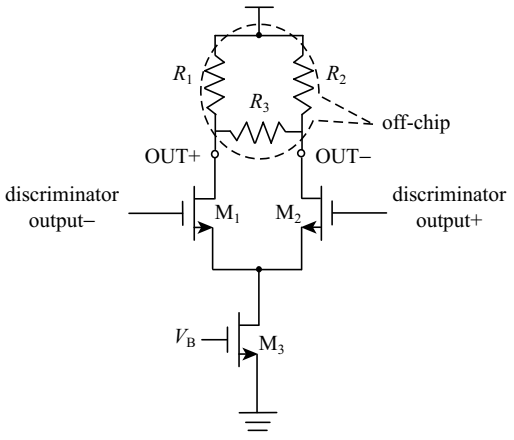

Fig. 5. Structure of the output driver.

3 Implementation and measurement

A five-channel prototype ASIC chip was implemented in a 0.13 μm CMOS process. Figure 6 shows a photograph of the fabricated ASIC chip. The chip size is 1.3 mm × 1.9 mm. For convenience of measurement, the readout ASIC chip is wire bonded to a printed circuit board (PCB), which can be connected to an evaluation board through the sockets. Ceramic packaging will be used to package the finalized chip in the future.

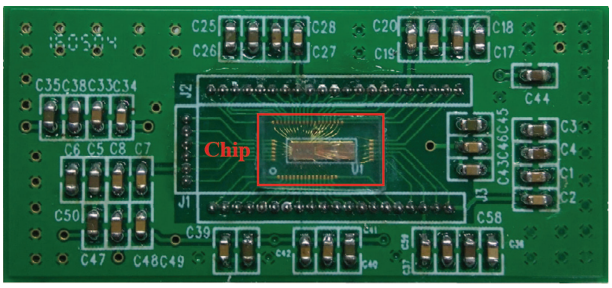

Fig. 6. (color online) Photograph of the ASIC chip.

3.1 ASIC chip measurement

The signal shape from several APDs for nuclear resonant scattering experiments can be found from Ref. [8]. The leading edge transition time of the APD output signals is from 0.8 ns to 2.1 ns. To capture this fast signal, the time constant at an input node of the ASIC chip should be in the order of a few hundreds of picoseconds. The maximum sensor capacitance in our R&D project is 10 pF. If the ASIC input impedance is 50 Ω, the RC time constant of the input node is 10 pF×50 Ω=500 ps, which results in a sufficient bandwidth to receive the APD output signal. Therefore, our ASIC chip is designed with an input impedance of 45 Ω. However, the APD sensor does not require impedance matching (∼ 50 Ω). For this ASIC, no external resistors are used to adjust the actual input impedance.

The time measurement setup is shown in Fig. 7. The performance of the ASIC chip was evaluated by generating input current pulses, via applying voltage steps to the 1 pF injection capacitances integrated in the test board. First, the generator signal was attenuated by an attenuator. Then, this attenuated signal was divided by a power splitter. One signal was connected through an injection capacitance to the input pad of each channel as the test signal, and the other was the trigger signal. To guarantee the impedance matching to the power splitter, 50 Ω resistances were added in the input terminals of each injection capacitance [14]. A TEK AFG3252C signal generator was used to generate the step voltage signals with a rise time of 2.5 ns. The time differences between the trigger signal and the leading edge of each channel output signal and the pulse width of each channel output signal were recorded and analysed by a Lecroy WaveRunner 640 zi oscilloscope. For each channel, measurements were carried out for different test signal amplitudes, set using different attenuations from the attenuator. For each channel and for each input charge level, 1000 measurements of the output signals were recorded.

The output pulse width variations with respect to the input charge measured with the threshold ($V_{\rm TH}$) setting at 25 mV are shown in Fig. 8 for channel 1. The typical pulse width varyied from 1.8 ns to 3.8 ns for input charges from 30 fC to 342 fC, respectively. The charge information can be retrieved from the measurement curve of the output pulse width. This curve has a non-linear relation, and a maximum sensitivity for the lower charges is also observed. In order to efficiently use the charge encoding possibilities of the chip with an optimum resolution, the threshold level of the chip must therefore be tuned so as to maximize the sensitivity around the working point of a specific application.

In the case of leading-edge discrimination, the channel output pulse leading edge time $t_{\rm lead}$ is delayed by the time needed for the signal to reach the threshold value. This delay, the Time Walk $t_{\rm w}$, has to be corrected for. The event time $t_{\rm event}$ can be given by [10, 11]:

$$t_{\rm event} = T_{\rm lead} - t_{\rm w}(V_{\rm TH}) = t_{\rm lead} - f(t_{\rm width}, V_{\rm TH}), \qquad (3)$$

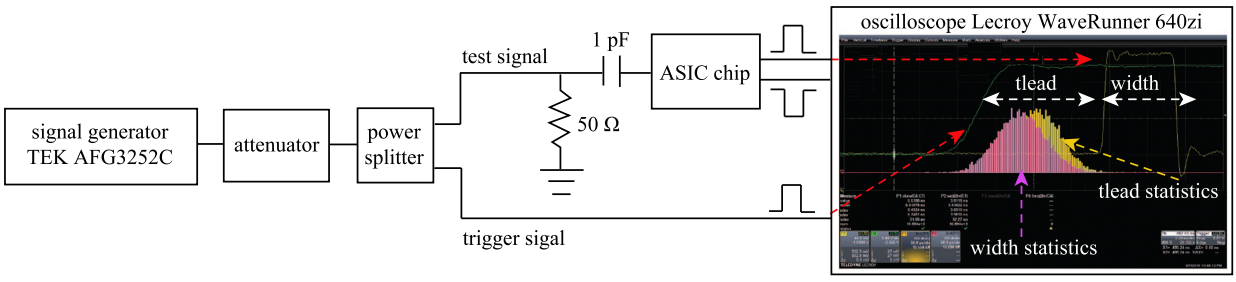

Fig. 7. (color online) Schematic of the setup for chip time measurement.

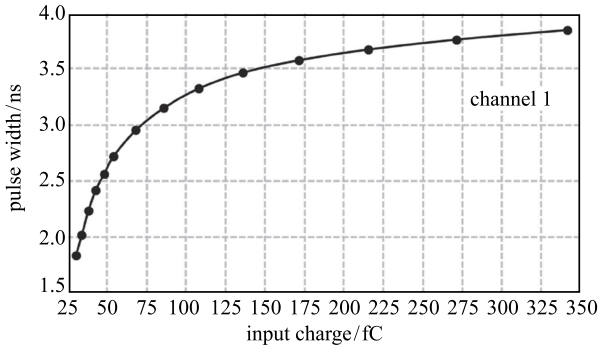

Fig. 8. Measured pulse width as a function of applied input charge for channel 1, with a threshold of 25 mV.

where $t_{\rm width}$ is the channel output pulse width. This method, applied off-line, permits a high-time resolution even for input signal amplitude varying on a large dynamic scale. All the $t_{\rm lead}$ time measurements acquired for the different input charges on channel 1 are shown in a scatter plot in Fig. 9(a) as a function of the measured pulse width. For the measurement, the threshold is set at 25 mV. The time walk variations are contained in clusters of less than 3 ns for input charges varying from 30 fC to 342 fC. The pulse width measurement can thus be used to correct for the time walk. This time walk correction procedure was applied event by event, leading to the scatter plot shown in Fig. 9(b). For each cluster of data points, the variations now correspond to the uncertainty in the time information that can be expected for a signal with such input charge.

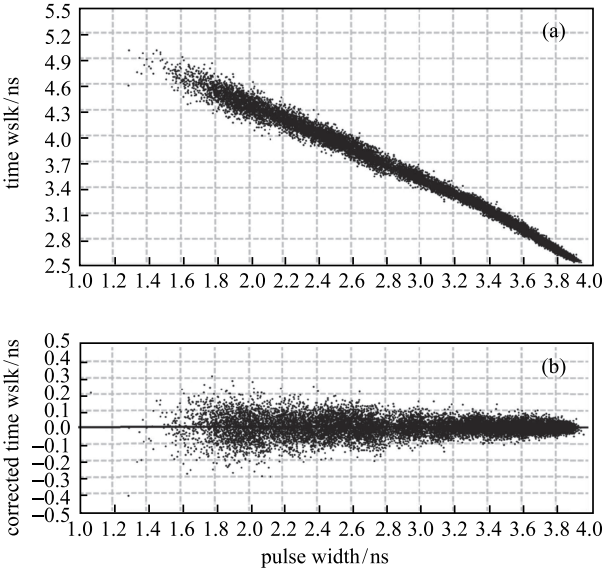

Fig. 9. (a) Measured time walk on the output pulse leading edge versus measured pulse width for channel 1; (b) time walk after off-line corrections applied to compensate variations of time walk with pulse width for channel 1.

To estimate the intrinsic time resolution of the circuit, the additional noise from the pulse generator and oscilloscope also has to be corrected. The measurement system time jitter has been measured with input charge from 15 fC to 342 fC, as shown in Fig. 10. This curve permits us to extract the function relating measurement system time jitter and input charge, and realize the measurement system time jitter correction procedure.

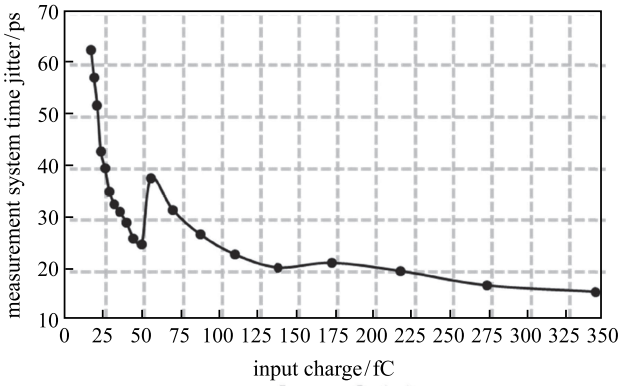

Fig. 10. Measurement system time jitter.

The measured time resolution (rms), the time resolution (rms) determined after time walk correction and the time resolution (rms) after both time walk correction and correction of the measurement system additional jitter noise are presented in Fig. 11 for channel 1, with $V_{\rm TH}$ set at 25 mV. The excellent time-resolution measured for an input charge Q can therefore be perfectly retrieved in the case of a system involving input signals varying on a large dynamic scale.

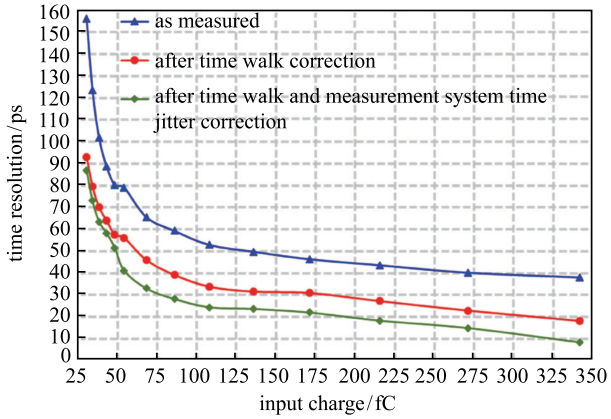

Fig. 11. (color online) Measured time resolution (rms) for channel 1, with threshold set at 25 mV, comparing measured time resolution, time resolution after time walk correction, and time resolution after both time walk and measurement system jitter noise correction.

After corrections are applied to compensate for the additional noise from the measurement system and to correct for the time walk variations due to pulse width variations, the intrinsic time resolution (rms) of channel 1 with specified threshold values is displayed in Fig. 12. Achievable resolutions are therefore directly dependent on the threshold level, which should be set according to the input signal shape, amplitude and dynamic range in the application.

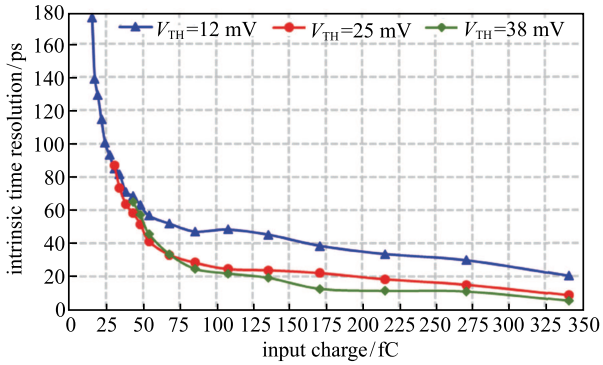

Fig. 12. (color online) Intrinsic time resolution (rms) of channel 1 versus input charge for the specified threshold values.

The intrinsic time resolutions (rms) attained at threshold level of 25 mV for channel 1 and channel 4 are shown in Fig. 13. The low charge signals exhibit a higher time uncertainty than signals with a higher charge. The intrinsic time resolution (rms) is better than 30 ps for high input signal charges (>75 fC) and better than 100 ps for low input signal charges (30–75 fC). The ASIC chip performance is detailed in Table 1. The measurement results demonstrate that the prototype chip has reached the design specifications.

3.2 Measurement with APD array sensor

Our APD array sensor is being designed by another group. Therefore, the prototype chip has been tested with a commercial APD array sensor (model: S8550-02, fabricated by Hamamatsu) at the 1W2B experiment station of Beijing Synchrotron Radiation Facility (BSRF). The S8550-02 is a monolithic 8×4 pixel structure with a photosensitive area of 1.6 mm $\times$ 1.6 mm and a terminal capacitance of 9 pF for each pixel. Five of the pixels were connected to the chip. The time measurement setup of the complete detector with sensor and readout chip is shown in Fig. 14. The RF signal from the accelerator storage ring served as the trigger signal. The time differences between the trigger signal and the leading edge of each channel output signal were recorded and analysed by a Lecroy WaveRunner 640zi oscilloscope. All the detector measurements were done with a threshold level set at 25 mV and an APD gain of 50.

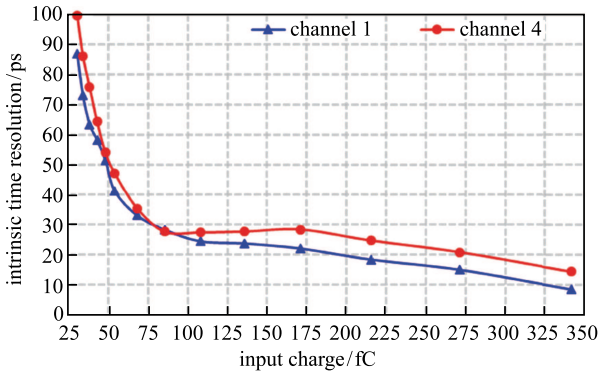

Fig. 13. (color online) Intrinsic time resolution of channel 1 and channel 4 for a threshold value of 25 mV.

The measured time structure of the beam bunches of BSRF using the developed APD array detector is presented in Fig. 15. The beam bunch structure has a hybrid fill pattern in which a specific single bunch is filled at a sufficient interval from other bunches. This single bunch is used to measure the time resolution of the developed detector. The measured bunch structure is consistent with the bunch current structure from the bunch current monitor, and proves the detector can work in a healthy state.

Table 1. Main performances of the prototype ASIC chip.

parameter	performance
process	0.13 μm CMOS
power consumption	<5 mW / channel (excluding the output LVDS driver consumption)
signal range	25–450 fC @ V_{TH} = 25 mV
discriminator threshold	$\geqslant$12 mV (15 fC)
time resolution (rms)	<30 ps @ input charge >75 fC; <100 ps @ 30 fC $\leqslant$ input charge $\leqslant$ 75 fC
count rate	$>1.2\times10^8$/s
input resistance	~45 Ω

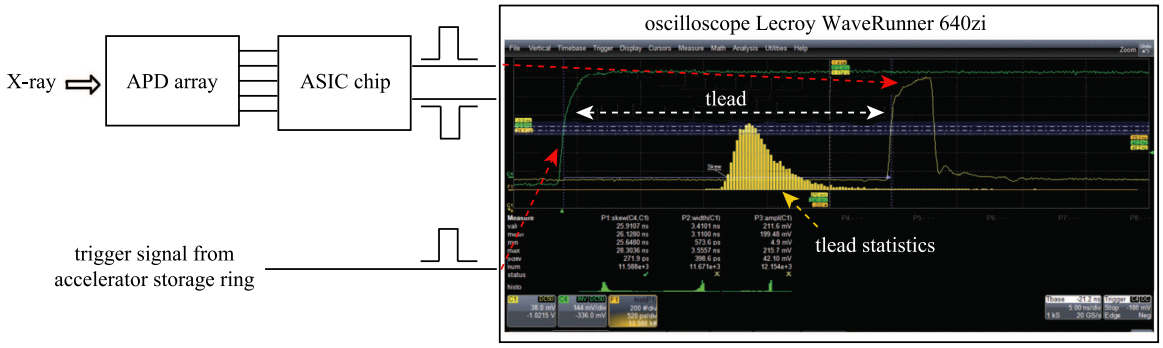

Fig. 14. (color online) Schematic of the setup for detector time measurement.

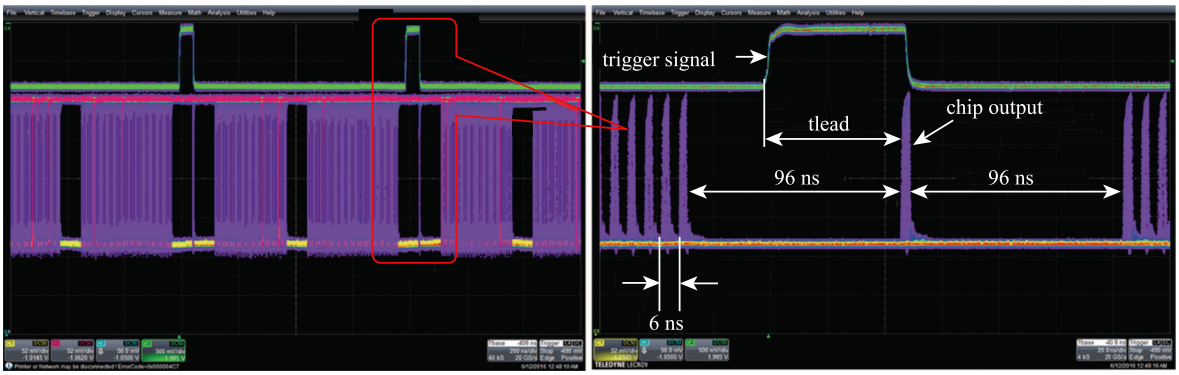

Fig. 15. (color online) Time structure of the beam bunch at BSRF: hybrid bunch structure with a singlet bunch.

The measured time resolution of the detector at 14.4 keV (equal to 32 fC input charge with the APD gain of 50) is displayed in Fig. 16. The time resolution (FWHM) is 350 ps, without any corrections. The S8550-02 is a "reverse type" APD [15, 16]. As compared with the reach-through design, the gain region is moved up to the front so that the active thickness is drastically reduced, while the depletion layer thickness is kept large. This makes the device specifically suited to couple with scintillators. It is not suitable to directly detect high energy X-rays. In the next step, our designed "reach-through type" APD array will be connected to the ASIC chip to form a practical detector for direct detection of high energy X-rays.

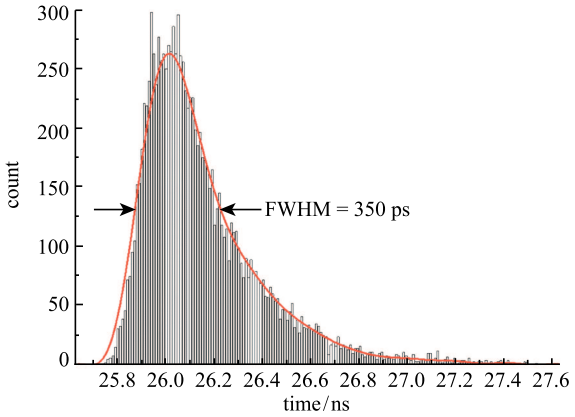

Fig. 16. (color online) Time resolution of the APD detector, with a threshold set at 25 mV.

4 Summary

In this paper, we have developed an ultrafast front-end ASIC chip for APD array detectors in X-ray time-resolved experiments. The present chip was fabricated in a 0.13 μm CMOS process, with four complete channels and one test channel, and fitted in an area of 1.3 mm× 1.9 mm. Pulse width measurement was used to do input charge measurement as well as time walk correction. After both time walk and measurement system jitter noise corrections, an intrinsic time resolution (rms) better than 30 ps for high input signal charges ($>$ 75 fC) and better than 100 ps for low input signal charges (30–75 fC) was achieved. The minimum detection threshold can be set at 12 mV, which is equivalent to an input charge

of 15 fC. The power consumption per channel is 5 mW, excluding the LVDS compatible output driver. A preliminary measurement with an APD array sensor (S8550-02) has also been done and a 350 ps resolution (FWHM), without any correction, was obtained. Further analysis and development to manufacture a practical detector is underway, including design of a 10 × 10 pixel "reach-through type" APD array and a ten-channel ASIC chip.

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